CONDUCTOR ANALYSIS
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Finer Printed Circuits...
Via Quantitative Data

Between The Conductors

From 1996 to 2005 Conductor Analysis Technologies, Inc. published a column in CircuiTree magazine related to printed circuit manufacturing process improvement and measuring printed circuit process capability, quality and reliability. This document is a compilation of the most relevant columns.

7.10 Impact of Copper Thickness on Quality - Part 1 - January-02
7.11 Impact of Copper Thickness on Quality - Part 2 - February-02
7.12 A Case for Collaborative Research & Development - March-02
8.1 Factory Design and Automation - April-02
8.2 PCQR^2 Industry Statistics - Introduction - May-02
8.3 PCQR^2 Industry Statistics - Outerlayer Conductor and Space - August-02
8.4 PCQR^2 Industry Statistics - 0.5 Ounce Innerlayer Conductor and Space - September-02
8.5 PCQR^2 Industry Statistics - 1.0 Ounce Innerlayer Conductor and Space - October-02
8.6 PCQR^2 Industry Statistics - Through Vias - November-02
8.7 PCQR^2 Industry Statistics - Soldermask Registration - January-03
9.1 Technology Erosion - March-03
9.2 The Impact of Conductor Width on Controlled Impedance - May-03
9.3 The effect of innerlayer processing on conductor height - July-03
9.4 Impact of panel thickness on registration - September-03
9.5 A Tool for Process Improvement - November-03
10.1 Highly Accelerated Thermal Shock (HATS) - April-04
10.2 Highly Accelerated Thermal Shock Results - July-04
10.3 Consumer Products - October-04
10.4 Can We Believe the Polls? - January-05
11.1 The Good, the Bad, and the Ugly - April-05
11.2 Standardized PCB Benchmarking Data - One Click Away - July-05

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume II • Issue 1**

THE IMPACT OF YIELD IMPROVEMENT ON PROFITABILITY

In the first three issues of *Between The Conductors*, test pattern defects were discussed in great detail. Defects were defined as "opens in conductors" and "shorts in spaces". A comparison of PWB panels with different feature lengths was made possible by the introduction of defect density, measured in defects per million inches of feature length (DEMIS). A model that was developed to predict first-pass product panel yield was also introduced. Repeating defects were defined, and the capability to censor them was discussed. In this issue, the impact of yield improvements on profitability will be estimated.

Evaluating the performance of the conductor formation process can be a challenging job. Production yields often exhibit large swings due to process variation and design complexity. Sometimes, an entire lot of panels may be rejected, while an entire lot of panels may be perfect at other times. Thus, using product to measure process capability, and to compare one process to another has limited potential. Until process performance is measured, it is difficult, if not impossible, to make improvements.

A solution to this dilemma is to process a set of "standard" panels, ones with significant conductor and space length. Using electrical test measurements to identify defects in the "standard" panels, conductor and space defect density as a function of feature width can be calculated and tracked. These data are used to calculate predicted first-pass panel yield on product. Results from these tests often provide insight into the sources of defects, allowing process changes to be made to improve conductor and space yield.

Purchasing new equipment such as developers and etchers, and new materials such as photoresists can be an expensive investment. Differences in initial system costs (capital, installation, etc.) and recurring costs (materials, labor, maintenance, etc.) could be outweighed by yield performance. Measuring performance before investing can provide the information needed to make the best decision. "Standard" panels are recommended to measure the performance of suppliers' equipment or materials, and to compare changes with the present process capability.

The following table illustrates the impact of yield improvement on profitability for a PWB manufacturer. The table shows incremental costs for a standard innerlayer process, and an improved innerlayer process. These figures are hypothetical, based upon estimates of process costs, production volume, and production schedule. The standard process produced an 80.0% first-pass panel yield. After inspection, 80.0% of the panels were acceptable, and 20.0% required repair. Half the panels needing repair were repaired successfully, and the rest were scrapped, to produce a final panel yield of 90.0%.

Assumptions	**Standard Process**	**Improved Process**
panel size	18" x 24"	18" x 24"
innerlayer panels / shift	400	400
shifts / day	3	3
first-pass yield	80%	84%
final yield	90%	92%

Material / Process Costs	**Standard Process**	**Improved Process**
1/1 copper clad FR4	$ 1.00	$ 1.00
preclean	$ 0.50	$ 0.50
photoresist material	$ 1.20	$ 1.20
apply photoresist	$ 1.00	$ 1.00
image resist	$ 3.00	$ 3.00
develop resist	$ 2.00	$ 2.00
etch copper	$ 2.00	$ 2.00
strip resist	$ 1.50	$ 1.50
inspect	$ 3.00	$ 3.00
repair	$ 0.60	$ 0.48
total cost / innerlayer	$ 15.80	$ 15.68
cost of scrap / shift	**$ 632.00**	**$ 501.76**

Period	**Number of Shifts**	**Savings**
Day	3	$ 390.72
Week	15	$ 1,953.60
Month	60	$ 7,814.40
Year	**720**	**$ 93,772.80**

First-pass panel yield was raised to 84.0%, and final panel yield was improved to 92.0% by using the improved innerlayer process. Using a modest volume of 400 innerlayer panels per shift, the cost of scrap in the standard process is $632.00 per shift. In the improved process, the cost of scrap is $501.76 per shift, a saving of $130.24 per shift. Projected to daily, weekly, monthly and yearly time periods, the savings are $391, $1954, $7814, and $93,773 respectively. However, many manufacturers have much higher production volume than illustrated here. The cost of scrap at a similar yield performance would be much higher, and the potential savings would be much greater for these higher volume manufacturers.

In addition to the quantifiable savings attributed to improved yield, there are other benefits afforded by conductor analysis technology. The understanding gained by careful study of the process can provide insight into causes of future "attacks" to yield, and provide tools for expeditious corrective action. Future issues of *Between The Conductors* will focus on the ability to measure and improve conductor width uniformity, and conductor height uniformity over the surface of the panels, from side-to-side on panels, and from panel-to-panel, which leads to extended capability and improved quality of the process.

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Between The Conductors

Conductor Analysis Technologies, Inc. **Volume II • Issue 2**

CONDUCTOR WIDTH UNIFORMITY: ISSUES AND PROCESS IMPACT

Previous issues of *Between The Conductors* concentrated on conductor and space yield, and how performance on test patterns relates to manufacturers' profitability. In this issue, conductor width uniformity is discussed with emphasis on defining, measuring, and improving quality.

Quality conductor formation processes form conductors of the desired width and height over the surfaces of panels, from side-to-side on panels, from panel-to-panel, and lot-to-lot, day in and day out. Every process, of course, will exhibit variation. The degree of variation that can be tolerated depends upon the specific application and the feature sizes used in the design. With technology advances requiring higher bandwidth and denser circuitry, designers are continually pressing for narrower conductors and spaces. As features become narrower, requirements on allowable defect sizes become stricter. For example, a small nick in an eight-mil line becomes an open in a three-mil line, while extraneous copper extending into an eight-mil space becomes a dead short in a three-mil space.

To achieve a specific level of controlled impedance, allowable conductor width tolerance decreases with narrower conductors. Assuming the control on conductor width to be comparable to that needed for impedance, a 10% controlled impedance requirement on an eight-mil line would allow a tolerance of ±0.8 mil. A three-mil line, on the other hand, would allow a tolerance of ±0.3 mil for the same impedance control, a much tougher job. Conductor width uniformity presents a challenge that PWB manufacturers as well as suppliers of materials and equipment to the industry will have to address.

Determining conductor width uniformity requires a measurement process with the resolution necessary to detect very small variations. Conductor Analysis Technologies, Inc. has developed an analysis process to convert a precision electrical resistance to an average conductor width and height, assuming a rectangular cross-section. The electrical resistance data are acquired from test patterns consisting of conductors of moderate length, constrained to one-inch-square modules over the panel surface. The combined spatial resolution and moderate conductor length of the test patterns provide an excellent tool to provide uniformity data.

A typical uniformity test entails processing a set of test pattern panels using the materials, equipment, and processes under study. Precision electrical resistance data gathered from the test pattern panels are processed with custom software to calculate conductor width and height. The analysis eliminates the data from defective conductors; those that are open and those that are shorted to a neighboring conductor. Only "good" conductors are used to calculate average conductor width and height. These data are processed further to provide uniformity information over the surface of panels, from side-to-side on panels, and from panel-to-panel. Statistics reported include the minimum, mean, maximum, standard deviation, capability potential index, and capability performance index for conductor width and height.

Many factors influence conductor width uniformity. The major steps in a print-and-etch conductor formation process, for example, that can impact uniformity include imaging, developing, and etching.

The imaging process begins with artwork and continues with photoresist application and exposure. The artwork, usually created on raster-scanned laser photoplotters, can impact uniformity. Film is available from many suppliers and in many grades, with different performance ratings of contrast and edge sharpness. Material properties, such as photoresist thickness and resist contrast can also influence uniformity. Factors such as exposure system intensity, intensity distribution, collimation, and hard or soft contact can all impact uniformity.

The job of the developer is to remove un-cured photoresist from the exposed panels. Developing must be accomplished cleanly, without leaving resist residues behind and without lifting the cured resist from the panel. The process is dependent on time, temperature, and concentration. Horizontal and vertical developers are available to the industry, each with their respective benefits and drawbacks. Both types require fresh developer chemistry to be delivered uniformly to the surface of the panels in order to accomplish the task. Neither of the two developers is perfect, or capable of fixing uniformity problems created during the imaging process.

Etching is the last major step in the conductor formation process that can impact conductor width uniformity. Once again, this step can not fix uniformity problems created up-stream, but it can adversely affect uniformity if not tuned properly. Like developing, etching is a process dependent on time, temperature, and concentration. Fluid dynamics play a major role in etching performance. Horizontal etching systems must overcome puddling problems on the top side and spray blockage by the conveyor system on the bottom side. Vertical systems often have a top-edge to bottom-edge variation, as well as a horizontal-to-vertical conductor width dependence.

Each of these steps in the conductor formation process can be measured and their impact on uniformity quantified. Once understood, changes to the process can be made to improve conductor width uniformity.

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Between The Conductors

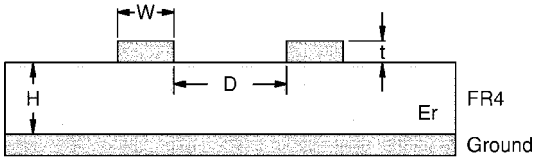
Conductor Analysis Technologies, Inc. **Volume II • Issue 3**

A STRATEGY TO IMPROVE ELECTRICAL PERFORMANCE

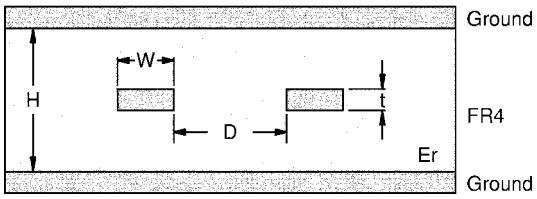
In the last issue of *Between The Conductors*, controlled impedance was discussed as one of the forces driving the PWB industry toward improved conductor-width uniformity requirements. In this issue a strategy is presented to achieve controlled conductor width, and correspondingly improved electrical performance.

Characteristic impedance, propagation delay, capacitance, and cross talk depend upon the material properties and geometry used in the manufacture of electronic circuits. Designers often refer to two classic mathematical models to predict circuit performance. External signal layers above a ground or power plane on multilayer boards can be modeled by a microstrip configuration, while internal signals placed between power or ground planes can be modeled by stripline relationships. In both configurations, dielectric constant, separation between signal and ground or signal and power, conductor width, and conductor thickness are factors affecting characteristic impedance.

Microstrip Configuration



Stripline Configuration



When considered separately, nominal manufacturing tolerances for each variable alone (with all other variables centered) are usually controlled well enough for the board to meet electrical performance requirements. However, when all tolerances collectively are allowed to vary, as in real manufacturing situations, achieving electrical performance requirements may be difficult. To achieve comparable impedance control, allowable variation is reduced as features become smaller. Controlling feature dimensions is an integral step, which is necessary, but not sufficient in achieving controlled impedance.

A strategy to achieve controlled conductor width is presented for print-and-etch innerlayers. The procedure is simple to implement but requires process characterization and optimization prior to the manufacture of product. The five-step approach is: 1) optimize the conductor formation process for conductor-width uniformity over the surface of the panels, from side-to-side on panels, and from panel-to-panel, 2) establish optimum conductor-width loss for dense circuitry, 3) determine differential conductor-width loss between conductors in dense circuit regions and isolated conductors, 4) apply a nominal artwork compensation to product to match optimum conductor-width loss, and 5) apply the differential compensation to individual isolated conductors requiring impedance control in product.

Conductor-width uniformity can be measured and improved by performing designed experiments that utilize multi-line or multi-pitch test pattern panels to determine sources of variation. Precision electrical resistance measurements taken from conductors on test pattern panels provide the necessary data to calculate conductor height, width and uniformity. Material, process, and equipment changes can be made to improve uniformity, based upon these data.

Optimum line-width loss, established from multi-line or multi-pitch test pattern panels, is defined as the reduction in width from the artwork width that results in the highest conductor and space yield. Conditions affecting conductor and space yield can be studied using designed experiments, leading to the optimum line-width loss.

Isolated conductors typically exhibit greater line-width loss than conductors in dense circuit regions. Differential conductor-width loss can be measured by processing test pattern panels with isolated conductors that are intermixed with test pattern panels with dense conductors.

Select artwork apertures for product equal to the desired finished conductor width plus the optimum line-width loss, which was established from test patterns in step number 2. For example, if the desired finished conductor width is 5 mils and the optimum line-width loss was 1¼ mils, choose an artwork aperture of 6¼ mils in diameter for these conductors.

Isolated conductors with impedance control specifications usually require a different artwork plotting aperture than those in dense circuit regions. If differential conductor-width loss was measured at ½ mil (isolated conductors measured ½-mil narrower than their counterparts in dense circuit regions), a 5-mil finished isolated conductor should be assigned an aperture of 6¾ mils in diameter, 1¾ mils larger than nominal.

Using this five-step approach, PWB fabricators can improve the electrical performance of circuits they manufacture, and extend their manufacturing capability to narrower features.

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Between The Conductors

Conductor Analysis Technologies, Inc. **Volume II • Issue 5**

PLATED COPPER UNIFORMITY

In the last issue of *Between The Conductors*, test pattern characteristics were discussed, and guidelines were presented to assist in the appropriate test pattern selection for specific applications. In this issue, the uniformity of conductors formed by a pattern plating process will be compared to those formed by a print and etch process.

Print and Etch

In a print and etch process, conductor height is controlled by the initial thickness of the vendor copper, and the cleaning process to which the vendor copper is subjected during circuitization. Variation in thickness is usually small in print and etch processes.

Print & Etched Panel

Capability Performance Indices with ± 20% Specification Limits

Artwork Size (mils)	Target Width (mils)	Number of Lines	Calculated Conductor Width (mils)						Control Indices	
			Min	Mean	Max	σ	LSL	USL	Cp	Cpk
4.00	3.00	350	2.27	2.73	3.11	0.167	2.40	3.60	1.20	0.66
5.00	4.00	350	3.28	3.73	4.13	0.159	3.20	4.80	1.68	1.12
6.00	5.00	351	4.29	4.72	5.12	0.163	4.00	6.00	2.05	1.48
7.00	6.00	351	5.27	5.73	6.10	0.166	4.80	7.20	2.42	1.87
Nominal Thickness (mils)	Target Height (mils)	Number of Modules	Calculated Conductor Height (mils)						Control Indices	
			Min	Mean	Max	σ	LSL	USL	Cp	Cpk
1.40	1.20	351	1.36	1.41	1.47	0.023	0.96	1.44	3.46	0.39

Table 1

Table 1 shows the conductor width and height summary for the top side of a panel manufactured by a print and etch process. The standard deviations for width and height reported in the table are typical for print and etch processes. Conductor width standard deviations often range between 0.1 mils and 0.2 mils, and conductor height standard deviation is usually below 0.03 mils.

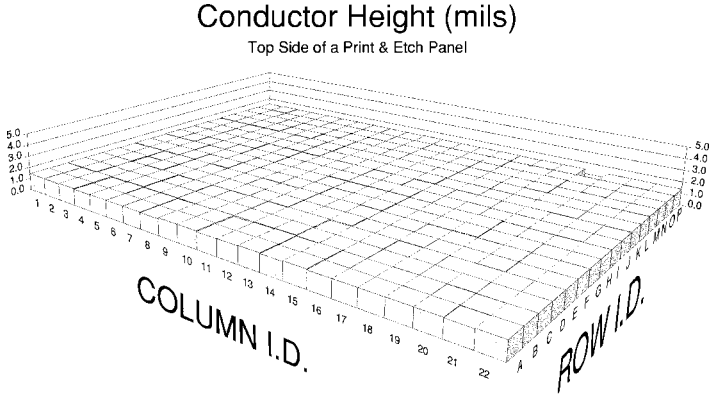

Figure 1

Figure 1 is a three-dimensional plot of the conductor height for this panel. Missing data in the three-dimensional plots occurs when less than three of the four conductors within a module are good. Lighter-shaded areas indicate thicker copper, while darker-shaded areas indicate thinner copper. This panel recorded a mean height of 1.41 ± 0.023 mils.

Pattern Plating

Table 2 reports the statistics for the top side of a pattern plated panel. The conductor widths are controlled slightly better than those in the print and etch panel, but the variation in conductor height was significantly greater. Conductor height in this case measured 2.94 ± 0.219 mils.

Pattern Plated Panel

Capability Performance Indices with ± 20% Specification Limits

Artwork Size (mils)	Target Width (mils)	Number of Lines	Calculated Conductor Width (mils)						Control Indices	
			Min	Mean	Max	σ	LSL	USL	Cp	Cpk
3.00	1.50	319	1.42	1.74	2.10	0.117	1.20	1.80	0.86	0.17
4.00	2.50	323	2.46	2.79	3.37	0.138	2.00	3.00	1.21	0.51
5.00	3.50	324	3.46	3.77	4.24	0.127	2.80	4.20	1.83	1.13
6.00	4.50	325	4.42	4.75	5.12	0.119	3.60	5.40	2.52	1.82
Nominal Thickness (mils)	Target Height (mils)	Number of Modules	Calculated Conductor Height (mils)						Control Indices	
			Min	Mean	Max	σ	LSL	USL	Cp	Cpk
1.40	2.50	325	2.51	2.94	3.80	0.219	2.00	3.00	0.76	0.10

Table 2

Rows A and B, and columns 1 and 2 in Figure 2 exhibited greater conductor height compared to the remainder of the panel surface. These extremely thick areas correspond to the perimeter of a set of panels that were held in a plating rack where higher plating current densities prevailed.

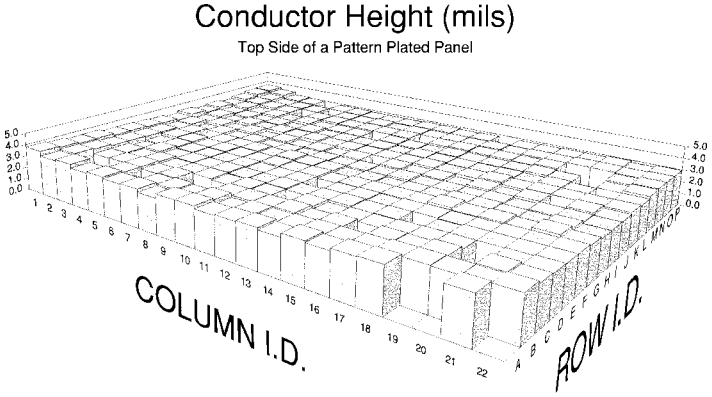

Figure 2

A non-uniform plating process can cause the copper to plate over the photoresist in some areas on the panels, leading to defects. In plated-through-hole applications, copper thickness in the hole often tracks with thickness on the surface. To minimize defects and improve quality, it is desirable to optimize plating thickness uniformity over the panel surface.

Summary

Conductor height on pattern-plated copper panels varies significantly more than on print and etch panels. The variation stems from non-uniform plating current densities over the surface of the panels. Plating cell geometry and plating chemistry can both impact thickness uniformity. Combining CAT Inc. technology with designed experiments, process engineers can measure and improve plated copper uniformity.

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Between The Conductors

Conductor Analysis Technologies, Inc. **Volume II • Issue 8**

AN EXPERIMENTAL DESIGN

In the last issue of *Between The Conductors*, the Process Figure of Merit was used to create the **Industry Data Base**. The results to date show a wide range in manufacturing capability, with room for improvement. In this issue, an experimental design is presented to study the exposure, developer and etcher processes used in the manufacture of innerlayers.

Goals

The goals of this experiment are to investigate the processing parameters in the exposure, developer, and etcher steps to determine their impact on conductor and space yield, and conductor uniformity. The measured responses include conductor yield, space yield, and conductor width standard deviation. Higher yield values and lower standard deviation values indicate improved performance.

Variables

The experimental variables investigated in this study are exposure dose, developer speed, and etcher speed. Each of these variables may have significant impact on the responses. All other settings are held constant at nominal values used to manufacture product.

Test Pattern

The process under investigation is used to manufacture product with a minimum line and space width of 4.0 mils. The multi-pitch test pattern with 4.0, 5.0, 6.0, and 7.0-mil lines and 4.0, 5.0, and 6.0-mil spaces is selected. Thus, the smallest features in the test pattern correspond to the operating limit for production.

Experimental Design

A 2^3 factorial design with a center point added is presented to determine the response of three factors at two levels. The experiment consists of two repetitions of ten panels each processed on different days according to the following design matrix:

Run Number	Panel Number		Exposure Level	Develop Level	Etch Level
	Day 1	Day 2			
1	7	6	-	-	-
2	5	3	+	-	-
3	3	10	-	+	-
4	8	1	+	+	-
5	2	7	-	-	+
6	9	5	+	-	+
7	4	8	-	+	+
8	1	2	+	+	+
9	10	9	0	0	0
10	6	4	0	0	0

The midpoint "0" is set at the current processing condition used to manufacture product. The process is operating at an exposure level of 50 mjoules, with developer and etcher speeds of 40 inches per minute. The developer speed of 40 ipm provides a 50% breakpoint. The high and low levels may be set according to the following table.

Level	Exposure Dose (mjoules)	Developer Speed (ipm)	Etcher Speed (ipm)
+	70	45	45
0	50	40	40
-	30	35	35

The extreme developer values, 35 ipm and 45 ipm, were established at the 40% and 60% breakpoints, respectively. The range of etcher speeds were selected to supply measurable differences in conductor width. By coincidence, the high "+" levels set for each factor create wider conductors, while the low "-" levels create narrower conductors.

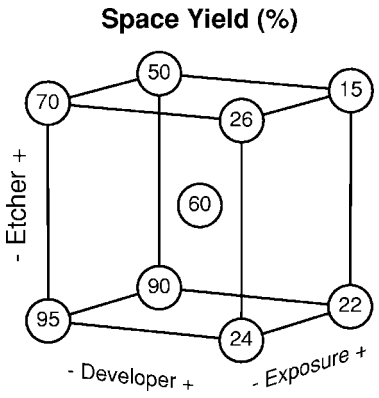
Process Panels

Panel identification numbers, inscribed in the panel border, are randomly assigned to panels in each replication to minimize systematic bias. The panels are to be processed in panel-number sequence.

Analyze Results

After both replications of the panels are completed, precision electrical testing and analysis by CAT Inc. will provide the necessary statistics to determine the responses for each run. The main effects and interaction effects may then be determined to establish the relative impact each variable imparts on quality, and provide direction on process change to improve quality.

Example results for 4.0-mil space yield is illustrated in the figure below. The response of each run is reported in the circle at the midpoint and each corner of the cube. The data suggest that space yield could be improved by slowing the developer and etcher speeds, and decreasing exposure, compared to the current manufacturing settings, indicated at the midpoint. Conductor yield and conductor width standard deviation responses would have to be considered before changes to the process could be recommended.



Summary

An experimental design is presented to investigate the imaging, developing, and etching steps in the manufacture of innerlayers. The experiment uses 20 multi-pitch test pattern panels in two replications of a 2^3 factorial design to ascertain the main effects and interaction effects of exposure dose, developer speed, and etcher speed on conductor yield, space yield, and conductor width standard deviation. Applications of designed experiments of this type can provide process engineers with the data necessary to extend manufacturing capability and improve product quality.

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Between The Conductors

Conductor Analysis Technologies, Inc. **Volume III • Issue 5**

CAPITAL EQUIPMENT PURCHASES

Advances in the electronics industry are compelling board-level manufacturers to form narrower lines and spaces on thin-core innerlayer substrate materials at high yields to compete in the marketplace. Given these requirements and the realization that their existing equipment falls short when attempting to build these products, manufacturers are replacing older equipment with new, advanced equipment.

Equipment purchases for the printed circuit industry are costly. When considering equipment purchases, PWB manufacturers often consider the purchase price, facilities' preparation, installation, maintenance, and operating costs as part of their return-on-investment analysis. Sometimes, beta-site installations are implemented to investigate the performance of new processes prior to a commitment to purchase. However, these arrangements are also costly to the PWB manufacturer, because they require facilities' preparation, installation, and the commitment of engineering staff and valuable floor space.

For QLP Laminates Inc., of Anaheim, CA, the time had come to replace a develop-etch-strip (DES) line for their innerlayer process. Because their product mix requires narrower lines and spaces with increased width control, the engineering staff decided to benchmark six DES lines from three manufacturers prior to purchase. The results from the performance benchmark tests would be included in their standard decision-making process, which typically includes purchase price, installation, maintenance, operating expenses, and vendor support. These performance evaluation tests would provide quantitative performance data that have not been available in the past. The DES vendors should recognize that both cost and performance are important to the PWB manufacturer. While the best-performing DES line may not be selected because of other considerations, a poor-performing DES line will not likely be considered for purchase.

Qualification Procedure

Planning and coordination of the qualification procedure are important factors that the PWB manufacturer's engineering staff must consider in the product performance evaluations. Potential vendors should be notified in advance of the tests, so that they have adequate preparation time to process the panels in their own R&D facilities, or at their customer installation sites. In the case of DES evaluations, delays in processing imaged panels can adversely affect the results, and lead to erroneous conclusions.

The engineering staff at the PWB manufacturer selected the multi-pitch test pattern with 4.0-, 5.0-, 6.0-, and 7.0-mil lines separated by 4.5-, 5.5-, and 6.5-mil spaces, respectively. This pattern is a good choice because it can be manufactured with reasonable high yield, and provides data that is used to calculate conductor and space defect density, and conductor width and height uniformity. Thus, the impact the DES lines have on yield and uniformity can be investigated by these tests.

The PWB manufacturer supplied 15 panels for each of the DES lines under consideration. The multi-pitch test pattern was imaged in photoresist on the panels, and the panels were shipped to the respective DES vendors (or a customer installation site) for processing. Five of the panels were to be used to set up the equipment. The completed panels were shipped to CAT Inc. for testing and analysis, and the *Analysis Reports* were shipped to the PWB manufacturer, with individual copies sent to the respective DES vendors.

Results

The test results are summarized here in terms of conductor and space defect density, and conductor width uniformity. The *Analysis Reports* include much greater detail about the process than is presented here. The six DES lines are identified in each of the following tables as 'A' through 'F'. Vendors 'B', 'C', 'E', and 'F' supplied 10 panels for testing, while Vendors 'A' and 'D' supplied 9 and 7 panels, respectively.

Conductor defect density, reported in defects per million inches (DEMIS), is summarized in Table 1. "Opens" in conductors cause increased conductor defect density. In all cases, repeating defects, which are usually created during the imaging process, were censored from the data. Repeaters are defects that affect the same feature in most, or all of the panels processed. In this case, the censoring level was set at 100 percent, which requires that the defect must occur in every panel within the set to be censored.

Target Line Width (mils)	A	B	C	D	E	F
3.0	782	613	54	208	164	**45**
4.0	296	82	27	26	27	**0**
5.0	113	46	28	26	37	**18**
6.0	145	28	9	0	84	**0**

Table 1. Conductor Defect Density (DEMIS)

Significant differences were observed in conductor defect density among the six DES lines. Vendor 'F' recorded the lowest defect density, with Vendor 'C' second best. Vendor 'A' recorded the highest defect levels.

Space defect density is reported in Table 2. "Shorts" between the conductors contribute to increased space defect density. Vendor 'C' recorded the lowest space defect density of the six DES lines investigated. Vendor 'A' had significant difficulty clearing the 5.5-mil space, but performed reasonably well at the 6.5- and 7.5-mil space widths.

Target Line Width (mils)	A	B	C	D	E	F
5.5	12943	398	**28**	331	268	222
6.5	125	271	**0**	307	215	112
7.5	31	160	**9**	148	85	56

Table 2. Space Defect Density (DEMIS)

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Treatment non-uniformity can often account for increased defect levels. The results for Vendor 'A', for example, show that the frequency of "shorts" in the 5.5-mil target space width is inversely related to line width loss. Areas on the panels with approximately 1-mil line loss had a very low frequency of shorts in the 5.5-mil spaces, while areas with approximately 0.0-mil line loss had a very high frequency of shorts in the 5.5-mil spaces. Thus, non-uniformity not only affects electrical performance by increasing impedance variation, but can also reduce yield.

Target Line Width (mils)	A	B	C	D	E	F
3.0	0.37	**1.74**	1.59	0.73	1.60	0.75
4.0	0.44	**2.04**	2.03	0.94	2.01	0.99
5.0	0.58	**2.50**	2.53	1.18	2.51	1.25
6.0	0.72	**3.43**	3.17	1.47	3.19	1.49

Table 3. Conductor Width Uniformity (C_p)

Table 3 presents conductor width uniformity in terms of the capability potential index (C_p). This index is defined as the difference between the upper and lower specification limits, divided by six standard deviations. The specification limits for these data were set at ±20 percent of the target conductor width. These data show that Vendor 'B' exhibited the best uniformity, with Vendors 'C' and 'E' tied for second best. Vendor 'A' displayed the poorest uniformity.

Summary

Equipment purchases are expensive investments that merit considerable investigation prior to commitment. In addition to the commonly used criterion such as purchase price and the costs associated with delivery, shipping, facilities' preparation, installation, maintenance, operating and vendor support, a performance evaluation will ensure that the equipment has the necessary capability to manufacture the intended products. If the overall cost of a system does not include a performance factor, a system that appears to be the best choice financially, may cost significantly more in terms of yield and uniformity penalties.

A quality innerlayer process must form conductors at high yield, uniformly over the surface of the panels, from side-to-side on the panels, and from panel-to-panel. Additionally, today's technology requires very thin materials be used for innerlayers. Often, the solutions to material transport impede treatment uniformity due to shadowing, a condition where the transport rollers block the chemical spray. Therefore, equipment performance evaluations are more important today then ever before.

In the performance evaluation discussed here, significant differences were measured among the six DES lines. In some cases, non-uniform treatment by the processing equipment contributed to increased defect levels. At the time of this writing, the engineering staff at QLP Laminates, Inc., reported their decision to purchase the DES equipment from Vendor 'C'. In addition to the commonly used return-on-investment factors, the performance of this DES line was second-best in conductor defect density, best in space defect density, and tied for second best in conductor width uniformity.

Acknowledgment

Conductor Analysis Technologies, Inc. would like to thank Valentina Perakh, Bob Keally, David Hollinsworth and Ken Lagemann of QLP Laminates Inc., Anaheim, CA for their contributions to this issue of Between the Conductors.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume III • Issue 7**

CORRELATION OF ELECTRICAL AND OPTICAL MEASUREMENTS

Introduction

Using proprietary analysis techniques, electrical resistance measurements from the conductors in test patterns provide the data to calculate average conductor width and average conductor height. These data are extremely useful in determining the uniformity of the circuitization process. The data collected from a standard 10-panel set of test patterns includes statistics from approximately 28,000 measurements.

One of the most common methods of determining conductor width and height is from optical measurements of cross-sections. This issue of *Between The Conductors* examines the correlation between the two methods.

Background

The test patterns consist of one-inch-square modules, covering the surface area of the panels. Each module contains four conductors separated by three spaces, forming a serpentine-shaped pattern over the area. The analysis of the precision electrical resistance data provides an average value for width for each conductor within each module, and an average value for conductor height for each entire module. The model that is used to calculate conductor widths assumes each conductor has a rectangular cross-section, averaged over the length of the conductor in the module. Thus, variations in width and height that may occur over the length of the conductors are averaged, and the extremes are not recorded.

In contrast, cross-sections examine specific parts of the conductors. Variations in width or height that may occur over the length of the conductor do not affect the values measured at the specific section under examination, and may go un-noticed. The section under examination may have average values for width and height, or values that are one, two, or more standard deviations from the averages. It is highly unlikely to section at a minimum or a maximum value, but the probability of taking the cross-section at locations "off the mean" is reasonable.

Cross-section Data

Cross-section measurements of conductors were provided by Tony Lentz of NTI, Colorado Springs, Colorado. Thirty-six cross-sections were examined in this study from a six-layer supplier qualification panel. The two outerlayers had conductors that were nominally 4.0-, 5.0-, 6.0-, and 7.0-mils in width, while the four innerlayers had conductors that were nominally 3.0-, 4.0-, 5.0-, and 6.0-mils in width. The innerlayers were formed by a print and etch process, while the outerlayers were formed by a print, plate and etch process.

Samples were taken from six modules near the center of each of six different panels. Three optical measurements were made for each conductor in the module: the width at the top, the width at the bottom, and the height of the conductor. Four hundred thirty-two cross-section measurements were provided to CAT Inc., with a reported measurement accuracy of ± 0.05 mils.

Correlation

First, conductor width and height were calculated from the electrical resistance data for each individual module corresponding to those that were cross-sectioned. Next, the weighted average width for each conductor was calculated from the optical measurements. The weighted average adjusts the actual trapezoidal shapes of the conductors into equivalent rectangular cross-sections. Since the sides of the conductors were concave, the values measured at the top of the conductors were closer to the average cross-section width than the values measured at the bottom. For innerlayers, the weighted average was calculated by:

$$W = (2 * top + bottom)/3$$

while the weighted average for the outerlayers was calculated by:

$$W = (3 * top + bottom)/4$$

These expressions were established from the "typical" cross-section photos that were provided by Mr. Lentz.

Next, the calculated conductor widths (from resistance data) were plotted against the weighted averages calculated from the cross-section data. Figure 1 shows these results from the innerlayers. These data are highly correlated (R^2=0.996), with widths measured from cross-sections averaging approximately 0.1 mils wider than those calculated from resistance.

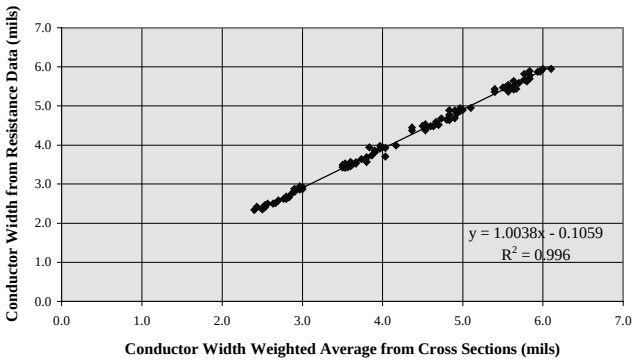

Figure 1. Innerlayer Conductor Width Correlation

Results for outerlayer conductor widths are shown in Figure 2. These data are highly correlated as well (R^2=0.964), with conductor widths measured from cross-sections averaging approximately 0.45 mils wider than those calculated from precision resistance data. This larger difference, observed between the cross-section and resistance methods, may be due to greater variability in width over the length of the features compared to the innerlayer conductors.

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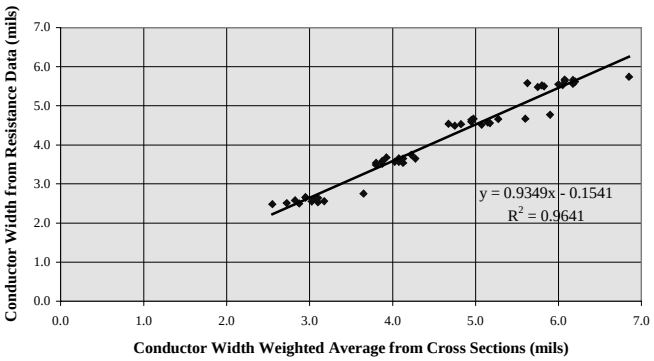

Figure 2. Outerlayer Conductor Width Correlation

Calculated from resistance measurements, Figure 3 shows the innerlayer conductor height plotted against conductor height measured from cross-sections. These data are nearly uncorrelated (R^2=0.127). The conductor height on the innerlayers had very small variations (from the electrical resistance results). Bars representing the reported accuracy of cross-section measurements (± 0.05 mils) are shown in the X-direction. In essence, the conductor height variation was less than the accuracy of the cross-section measurement technique, which lead to the low correlation between the two methods.

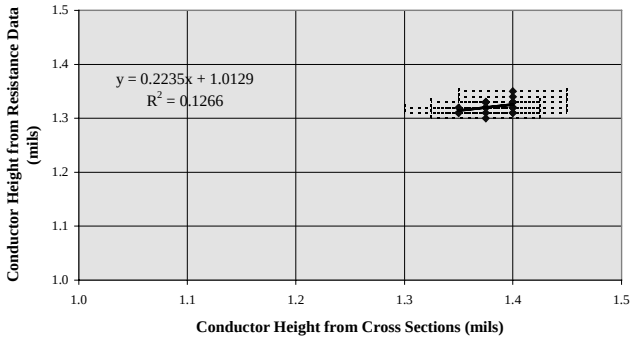

Figure 3. Innerlayer Conductor Height Correlation

Improved correlation between conductor height determined from cross-section measurements and resistance measurements was observed in the data from the outerlayers, as shown in Figure 4. In this case, the correlation coefficient was 0.828, with conductor height determined from cross-sections approximately 0.15 mils thinner than conductor height determined from resistance measurements. Again, bars are shown in the figure ± 0.05 mils about the cross-section measurements.

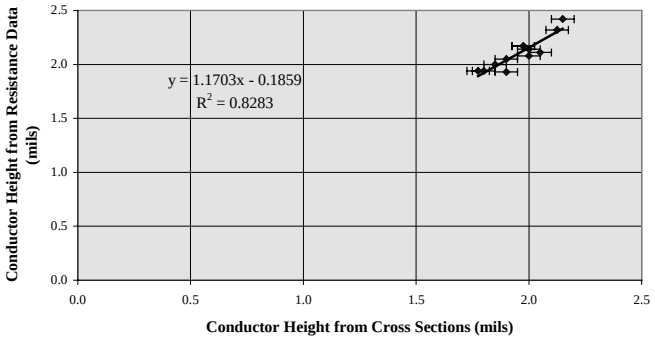

Figure 4. Outerlayer Conductor Height Correlation

Summary

Conductor widths and heights, which were calculated from electrical resistance data, were correlated with optical measurements made from conventional cross-sections. Excellent agreement was observed between the two methods. Both innerlayer and outerlayer conductor widths were highly correlated between the two methods, with correlation coefficients of R^2=0.996 and R^2=0.964, respectively. Conductor widths calculated from electrical resistance data were approximately 0.1 mils and 0.45 mils narrower than those from innerlayer and outerlayer cross-sections, respectively.

Innerlayer height was uncorrelated (R^2=0.127), primarily because the variation was smaller than the accuracy of the optical measurement. Outerlayer conductor heights showed good correlation (R^2=0.828), with electrical measurements approximately 0.15 mils greater than optical cross-sections.

Cross-sections and electrical resistance measurements complement one another in evaluating the circuitization process. Cross-sections are useful in determining the details of conductor shapes, and provide conductor width and height data, but they record a snapshot of the conductors at the location the section was taken. Thus, to gain an overall view of the process, many cross-sections may be required.

The electrical resistance method provides an average value for conductor width over the length of each conductor, and the average conductor height over the one-inch square module area. These data are readily available from the testing of specially designed test patterns, and provide valuable information to measure, track, and improve the circuitization process. Conductor and space defect density, and conductor width and height uniformity are quantified from the tests.

Acknowledgments

Conductor Analysis Technologies, Inc., greatly appreciate the contributions made to this issue by Tony Lentz, Richard Falat, and Jack McCreary of NTI, Colorado Springs, CO.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume III • Issue 8**

THE PAST… PRESENT… AND FUTURE

Introduction

Ten years have brought dramatic changes to the PWB industry. Environmental forces have accelerated the shift from solvent-based resists to aqueous resists. Alternatives to conventional electroless copper, which contains formaldehyde, are becoming more prevalent in the industry.

The electronics industry is continuously pressed toward higher density interconnection capability. Significant changes over the last ten years have resulted in narrower lines and spaces, smaller through-holes, and tiny microvias becoming commonplace. New technologies have been developed, not the least of which is sequential build, which takes full advantage of microvia routing ability. New materials, equipment, and processes have been developed to provide solutions to the problems associated with increased interconnection requirements.

Challenges to ensure functionality, performance, and quality appear along with this influx of miniaturization. Traditional methods include electrical test and optical inspection. These technologies are faced with challenges of their own, to keep pace with technological advances in PWB manufacturing. Both conventional electrical test and optical inspection are faced with tradeoffs of resolution, speed, and cost in their efforts to test and inspect narrower lines and spaces, and smaller pads placed on smaller grids.

An important change is beginning to take hold in the industry, which provides ways to measure and improve the circuitization process used in the manufacture of circuit boards. In addition to test and inspection of the finished product, manufacturers are improving the circuitization process, leading to higher quality products.

The Past

The PWB industry originated in the United States. With global markets and off-shore competition growing in the mid 1980s, many companies recognized the need to develop new capability, or face the realization that all manufacturing will take place off-shore. The October Project and the National Center for Manufacturing Sciences PWB Interconnect Program were two collaborative efforts designed to improve manufacturing capability. The participants in the NCMS program included the following: AlliedSignal, AT&T Bell Laboratories, Digital Equipment, IBM, Sandia National Laboratories, Texas Instruments, and United Technologies/Hamilton Standard Interconnect.

I was a member of the NCMS Imaging Team, and one of the representatives from AT&T Bell Laboratories. The goals of the Imaging Team included identifying current processes capable of manufacturing six-mil-pitch circuitry on large panels at high yield, and potential leap-frog technologies capable of four-mil-pitch circuitry.

At the time, team members were not aware of any process capable of achieving the desired yield. As part of the development efforts, we pursued tools to provide a quantitative measure of performance. The primary components of the tools were specialized test patterns, electrical test equipment, and analysis software.

As team members ran experiments at their respective facilities and supplier installations, the demand for testing outpaced the supply. Initially, a single, custom-designed, two-probe system was available for test pattern testing. Subsequently, commercially available two-probe systems were modified to provide additional testing capability, while a new system with a dedicated test head was added to the arsenal.

Testing continued to be a bottleneck! After the Imaging Team exhausted commercially available sources for suitable systems, Tim Estes lead a team at Sandia National Laboratories to develop a prototype system capable of testing 12" x 12" panels. The completed prototype outperformed existing systems in terms of speed, precision, and accuracy, but could not handle the larger 18" x 24" panels generally used in the studies. However, this system was used extensively by the Sandia team to measure and improve their manufacturing capability.

Each member company wanted one of these new full-sized high-performance test systems to expedite testing and improve productivity. However, this option was not economically feasible due to the cost of the system and budget constraints. None of the companies could afford one. As a solution to this dilemma, Tim and I offered to establish a new company that would provide testing and analysis services for the participating NCMS member companies and the commercial industry. Tim took a leave-of-absence from Sandia and I retired — this marking the beginning of Conductor Analysis Technologies, Inc.

The Present

Conductor analysis has changed considerable since those early days. Our third generation test system is two orders of magnitude faster, and one order of magnitude more precise than the original two-probe system. Our test pattern selection has grown from a total of eleven in those early days to over 4000. Our analysis software runs under Windows™, rather than DOS, and is faster and far more comprehensive than the original DOS version.

Recognizing that conductors are only one part of the picture, we have added new products to measure and improve the quality of vias and registration.

During this same time period, major restructuring within the industry has resulted in fewer captive PWB shops in the United States. Most of the companies participating in the NCMS program have either sold or closed their PWB shops,

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while the large commercial shops have grown larger during the same period.

In the past, manufacturers had struggled with quality issues, which included yield, uniformity, and reliability. Today they are faced with the same problems, but on a different scale. The forces within the electronics industry that are requiring higher density are causing manufacturers to operate at the knee of the capability curve. Sometimes yields are acceptable, or even high. Then, for some unknown reason, the bottom drops out and yields plunge. Most of us have observed this phenomenon throughout our careers.

One of the factors contributing to this recurring problem is an inadequate understanding of the manufacturing process. It's difficult, if not impossible, to improve something you can't measure! Without the necessary tools at hand, process engineers who are given the responsibility to solve these issues will continue to struggle for a lasting solution.

The Future

Lines and spaces will continue to get narrower. Through-holes, blind and buried vias, as well as their associated lands will continue to shrink in size. The result will be greater interconnection capability within smaller packages. However, PWB manufacturers will continue to push for product to be manufactured on larger panels, rather than smaller ones, because of increase throughput. These trends require lower conductor and space defect density, and lower microvia defect density on features that are smaller, and inherently more difficult to manufacture.

The costs associated with test and inspection will become a larger fraction of the total cost of the finished circuit board. These costs may be off-set partially by those manufacturers who place resources on the task of understanding and improving the process. A full understanding of the process can lead to lasting improvements in yield, quality, and reliability while providing an ongoing competitive edge. Indeed, the future rests with all of us in the industry. Maintaining a perspective on the future while solving the near-term problems will help PWB manufacturers meet the challenges of miniaturization and provide high quality, high reliability boards.

Acknowledgments

As a member of the NCMS imaging team from 1991-1994, I was associated with some of the finest people in our industry. It was a privilege to work with them and I offer special thanks to Gene Allen, Ron Evans, Jerry Fefferman, Ray Rust, David Au, Dick Kovacs, Les Connally, Anita Murray, Bob Carhart, Natalie Feilchenfeld, Tim Estes, Gerald Cessac, Moffatt Kennedy, Ray Timmons, Ray Fawcett, and Steve Goldammer.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume III • Issue 9**

DEFECT DENSITY

Introduction

Printed circuit board manufacturers are not creating all its circuitization at 100 percent yield – if they are, they shouldn't be! The demands of the printed wiring board marketplace are always pushing toward narrower lines and spaces as one of the solutions to achieve higher density. If a manufacturer is operating at very high circuitization yields, then there is a market with narrower features that has gone untapped, which could expand its business, add profits, and position the company for future technologies.

Many times however, when a new design is quoted for manufacture that has narrower features than are normally manufactured, the manufacturer suffers severe yield penalties until the learning curve is surmounted. The solution may include the diligence of process engineers on an ongoing basis, until new processes are implemented with greater capability than are currently in place. The manufacturer may suffer severe financial losses on that job, because it is beyond its manufacturing capability.

Rather than taking on more challenging work than accustomed without the proper knowledge and understanding, manufacturers have the ability to measure capability, understand their processes, and predict the impact that narrower lines and spaces will have on yield. The first element in this understanding is ***defect density***. Expressed in defects per million inches (DEMIS), this metric normalizes the impact defects have on conductors and spaces.

Unfortunately, the defect density for a process is not constant with time, but rather is affected by the materials, equipment, and processing conditions of the moment. During the endeavor to measure defect density, manufacturers will discover which conditions improve performance and which ones do not. They may find that some parameters are under control, but that others are not. *It's difficult – if not impossible – to improve something you can't measure*. Just the action of measuring defect density can lead to improved quality.

Test Patterns

The circuitization process should be characterized by manufacturing test patterns, rather than product. Test patterns, designed specifically to measure the quality of the circuitization process, offer advantages over product that include the following:

- Variety of feature sizes is available to explore the process limits.
- Individual conductor and space lengths are on the order of those found in product.
- Total conductor and space lengths in test panels provide a good statistical basis for defect density while processing a minimum number of panels.
- Maps of defects that occur in test panels assist in categorizing defects as process-limited, systematic, repeating, and random, and provide information that may lead to their cause.
- Conductor and space defect density, calculated from data collected from test patterns, may be used to predict first-pass yield on product.
- The data from test patterns provides direction to extend capability and improve quality.

Model

A model has been developed to measure conductor and space defect density from test pattern panels. Defects are often Poisson-distributed, but for them to fit the model, they must be random and independent. Repeating defects, which are caused during the imaging process by dirt, dust, or damaged artwork, are not independent and must be censored from the data. Likewise, events affecting every feature within a module, caused by improper handling or faulty conveyorized transport systems, are not independent and must be censored as well. Although these events and repeating defects are censored, their impact will still be felt by product, and to the extent that they exist will lower yield below the model's predictions.

To apply test pattern results to product, "opens" and "shorts" defects are treated separately. "Opens" are defined as defects in conductors, while "shorts" are defined as defects in spaces. Separating the defects in this manner allows statistics from any conductor within the test pattern to be combined with those from any space within the test pattern to predict performance on product.

The Poisson model defines the probability of having the number of defects, k, in conductor length l by the following equation:

$$P(l,k) = \frac{(\lambda\, l)^k}{k!} e^{-\lambda l} \tag{1}$$

where:

$$\lambda = \text{ defect density} \tag{2}$$

The term "yield" may be derived from Equation (1) when k=0, i.e., the probability of zero defects.

$$\frac{Y}{100} = P(l,0) = \frac{(\lambda\, l)^0}{0!} e^{-\lambda l} = e^{-\lambda l} \tag{3}$$

Thus, "yield" can be defined by the following equation:

$$Y = 100\, e^{-\lambda l} \tag{4}$$

Solving Equation (4) for λ provides the following expression for defect density:

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$$\lambda = \frac{-ln\left\{\frac{Y}{100}\right\}}{l} \quad (5)$$

where:

Y = feature yield

l = length of individual features

Conductor Defect Density

To determine conductor defect density, a set of test pattern panels must be processed, the conductors in the patterns tested for "opens", and Equation (5) applied with the following definitions:

$$\lambda_C = \frac{-ln\left\{\frac{Y_C}{100}\right\}}{l_C} \quad (6)$$

where:

λ_C = conductor defect density

$Y_C = 100\left\{\frac{\text{number of good conductors}}{\text{total number of conductors}}\right\}$

l_C = length of individual conductors

Space Defect Density

Similarly, the space defect density may be determined by testing the same set of test panels for "shorts" in the spaces, and applying the following equation:

$$\lambda_S = \frac{-ln\left\{\frac{Y_S}{100}\right\}}{l_S} \quad (7)$$

where:

λ_S = space defect density

$Y_S = 100\left\{\frac{\text{number of good spaces}}{\text{total number of spaces}}\right\}$

l_S = length of individual spaces

DEMIS

Conductor defect density is calculated for each conductor width in the test pattern, and space defect density is calculated for each space width in the test pattern. Defect densities are tabulated in the analysis results and expressed in *Defects per Million Inches* (DEMIS).

Table 1 displays example results from tests of ten panels. There were no repeating defects in this set of data, but one "opens" event and two "shorts" events lowered the feature count accordingly. The results show that the 4.5-mil target space width is the most difficult feature to manufacture, with the 5.5-mil target space next.

The following expression is used to calculate DEMIS:

$$DEMIS = \frac{-10^6 \ln\left\{\frac{Y}{100}\right\}}{l} \quad (8)$$

where the feature length, l, is measured in inches.

Summary

When the circuitization process is investigated by using standardized test pattern panels, the measurements acquired reflect process capability, which are not confounded by variations in product complexity. Thus, an understanding of the process can begin initially by benchmarking, and continue by tracking performance. The variations that occur shift-to-shift, day-to-day, or week-to-week, for example, will indicate the control (or lack of control) in the process, and provide data to improve quality.

The first measures of quality gained by implementing programs such as these are conductor and space defect density. These metrics normalize defects to feature length, which allow them to be applied to yield predictions on product. The data gathered by processing test patterns with features that are smaller than those on product can provide the information to predict product yield. Considering these predictions, manufacturers can provide quotations for designs with narrower features than are currently in production, with assurance that they can be manufactured, or alternatively – decline to quote.

In the next issue of *Between The Conductors*, the defect density data will be applied to a model to predict first-pass panel yield on product.

Artwork Feature Size (mils)	Target Feature Size (mils)	Feature Type	Feature Count	Defect Type	Defect Count	Number Good	Feature Yield (%)	DEMIS
4.5	3.5	Line	7039	Open	3	7036	99.96	25
3.5	4.5	Space	7038	Short	240	6798	96.59	2045
5.5	4.5	Line	7039	Open	1	7038	99.99	8
4.5	5.5	Space	7038	Short	25	7013	99.64	212
6.5	5.5	Line	7039	Open	2	7037	99.97	17
5.5	6.5	Space	7038	Short	2	7036	99.97	17
7.5	6.5	Line	7039	Open	0	7039	100.00	0

Table 1 - Example Defect Density Results

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume III • Issue 10**

PREDICTING YIELD

Introduction

In the last issue of *Between The Conductors*, the concept of defect density was defined and discussed. By measuring conductor and space defect density from test patterns, manufacturers gain a fundamental understanding of the manufacturing process, which enables improvements in yield and quality to be made. In this issue, the defect densities discussed in the last issue are used to predict yield on product, which will provide manufacturers with the information necessary to determine their ability to manufacture narrower features than are currently in production.

First-Pass Yield

The definition of yield may vary from one manufacturer to the next. For the purposes of predicting yield, we define first-pass panel yield on product as:

$$Y_{fp} = 100 \left\{ \frac{\text{number of defect - free panels}}{\text{total number of panels processed}} \right\} \qquad (1)$$

where $\boldsymbol{Y_{fp}} \equiv$ first-pass panel yield on product.

Notice that the definition applies to panels, not boards. Further, the term defect-free panels means panels with no "opens" or "shorts" prior to the repair process.

Procedure

The defect densities, which are established from the manufacture, test and analysis of test patterns, are combined with the conductor and space length on production panels to predict yield.

The following steps comprise the procedure to calculate first-pass panel yield on product:

1. Process test pattern panels with the materials, equipment, and processes under investigation.
2. Electrically test the panels for "opens" in the conductors and "shorts" in the spaces.
3. Calculate conductor and space defect density.
4. Estimate feature length on product.
5. Determine fraction yield on product due to "opens".
6. Determine fraction yield on product due to "shorts".
7. Calculate first-pass panel yield.

Fraction Yield on Product Due to "Opens"

Fraction yield on product due to "opens" is calculated from the "opens" defect density determined from test patterns, and the estimated conductor length on product. For specific designs, manufacturers can directly measure conductor length on product. For the more general case, conductor length may be estimated from the panel size, panel active area, utilization of panel active area, and conductor pitch. Knowing these parameters, the following equation is used to estimate the total conductor length on a production panel:

$$L_C = \frac{2 A_A U_A}{P} \qquad (2)$$

where $\boldsymbol{L_C}$ is the total conductor length on one production panel, $\boldsymbol{A_A}$ is the panel active area per side, $\boldsymbol{U_A}$ is the utilization of active area, and $\boldsymbol{P}$ is the conductor pitch. Typical values for an 18" x 24" panel are 300 square inches per side for active area, and 10 percent for utilization.

The fraction yield on product due to "opens" is calculated by:

$$Y_{fo} = e^{-\lambda_C L_C} \qquad (3)$$

where λ_C is the conductor defect density due to "opens" determined from test pattern panels and $\boldsymbol{L_C}$ is the total conductor length on both sides of one production panel.

Fraction Yield on Product Due to "Shorts"

The length of narrow spaces on product is always less than that of narrow conductors. For specific designs, manufacturers can directly calculate space length. To estimate space length for the general case, the space-to-conductor length ratio is used, typically 50 percent. The fraction yield on product due to "shorts" is calculated by:

$$Y_{fs} = e^{-\lambda_S L_S} \qquad (4)$$

and

$$L_S = \delta L_C \qquad (5)$$

where λ_S is the space defect density due to "shorts" determined from test pattern panels, δ is the space-to-conductor length ratio, and $\boldsymbol{L_S}$ is the total space length on both sides of one production panel.

Predicted First-pass Panel Yield

Predicted first-pass panel yield on product is calculated by:

$$Y_{fp} = 100\, Y_{fO}\, Y_{fS} \qquad (6)$$

where $\boldsymbol{Y_{fp}}$ is predicted first-pass yield on product, $\boldsymbol{Y_{fo}}$ is the fraction yield on product due to "opens", and $\boldsymbol{Y_{fs}}$ is the fraction yield on product due to "shorts".

Example results showing predicted first-pass yield on product are shown in Table 1. Statistics for each conductor in the test pattern are paired with each space in the test pattern. Feature length on product was estimated using Equation (2) and Equation (5), with an active area of 300 square inches per side, 10 percent utilization of active area, and a 50 percent space-to-conductor length ratio. The model predicts very high first-pass yield on product with target features of 6.5-mil lines and spaces. The 2,045 DEMIS recorded in the 4.5-mil target space drops the predicted yields to zero. Even the 212 DEMIS

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measured in the 5.5-mil target space imparts significant yield penalty. When the 5.5-mil target space is combined with the 6.5-, 5.5-, 4.5-, and 3.5-mil lines, the model predicts 59, 51, 50, and 42 percent first-pass yields, respectively.

Summary

By developing methods to quantify process capability that are independent of product, manufacturers of printed wiring boards can gain a fundamental understanding of the circuitization process. Unlike the *elastic yardstick* due to varying complexity of product, standardized test patterns, which are designed specifically to measure conductor and space defect density, provide data to improve quality, extend capability, and predict performance.

The knowledge gained from tests to measure process capability, combined with the models presented here, can provide manufacturers with the tools and data to predict first-pass yield on product. Information gained from these tests can be used as a basis for quotation of new designs having features narrower than are currently in production.

Artwork Width (mils)		Target Width (mils)		Estimated Feature Length on a Production Panel (inches)		Defect Density Determined from Test Patterns (DEMIS)		Predicted Fraction Yield due to		Predicted First-Pass Product Panel Yield
Line	Space	Line	Space	Line	Space	Opens	Shorts	Opens	Shorts	(%)
4.5	3.5	3.5	4.5	7,500	3,750	25	2,045	0.831	0.000	0.00
4.5	4.5	3.5	5.5	6,666	3,333	25	212	0.848	0.494	41.90
4.5	5.5	3.5	6.5	6,000	3,000	25	17	0.862	0.950	81.92
5.5	3.5	4.5	4.5	6,666	3,333	8	2,045	0.946	0.001	0.10
5.5	4.5	4.5	5.5	6,000	3,000	8	212	0.951	0.530	50.44
5.5	5.5	4.5	6.5	5,454	2,727	8	17	0.956	0.955	91.23
6.5	3.5	5.5	4.5	6,000	3,000	17	2,045	0.904	0.002	0.20
6.5	4.5	5.5	5.5	5,454	2,727	17	212	0.813	0.562	51.26
6.5	5.5	5.5	6.5	5,000	2,500	17	17	0.920	0.958	88.13
7.5	3.5	6.5	4.5	5,454	2,727	0	2,045	1.000	0.004	0.38
7.5	4.5	6.5	5.5	5,000	2,500	0	212	1.000	0.589	58.93
7.5	5.5	6.5	6.5	4,615	2,307	0	17	1.000	0.961	96.15

Table 1 - Example Predicted First-Pass Panel Yield

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume III • Issue 11**

A QUESTION OF RELIABILITY

Introduction

When new materials and processes are developed to manufacture PWBs, a question of reliability must be addressed to ensure high-quality, long-lasting products. Today's design rules are yesterday's design violations. I can remember when a 5-mil minimum clearance from one trace to the next was necessary to meet reliability specifications. To achieve that requirement, designs were created with larger clearances to allow for process variations. In contrast, designers today routinely develop designs with 5-mil lines and spaces, and use smaller features (4/4, 3/3, perhaps 2/2) when necessary.

There are many test programs in place to investigate the quality of products manufactured with new materials and processes. Accelerated aging techniques, which are used to subject test samples to harsh environments, are routinely used to predict the life expectancy of products. When subjecting test samples to controlled humidity, temperature and voltage bias, samples are forced to fail earlier than they would in actual use. Extensive modeling is applied to the set of samples, and the useful life is projected under expected operating conditions.

Traditionally, PWBs are continually gaining density by utilizing narrower lines and spaces, thinner layers, smaller holes, and recently, microvias. Sequential-build technologies are being developed and introduced to satisfy the thirst for higher density. With conductor spacing becoming narrower, separation between layers becoming thinner, and holes becoming microvias, the need for reliability studies will not go away. In fact, reliability studies are more important now than ever before.

In the past when feature sizes were larger, a 20 percent variation in feature size could result in a reduction of the designed space by approximately one mil. A 6-mil line and space technology would require the traces to be manufactured to 6.0 ± 1.2 mils. This may cause a 6-mil designed space to become a 4.8-mil space, with a minimum impact on the product reliability. Maintaining 20 percent control on the width of 3-mil lines requires that they be manufactured to 3.0 ± 0.6 mils, a much more difficult task to achieve. If the manufacturer could control the trace widths to this tolerance, a 3.0-mil designed space could range between 2.4 and 3.6 mils. With less control, the space may become dangerously narrow, leading to failures of products in field-use.

Reliability tests are often based upon a small set of samples that are manufactured with the same materials and processes intended for product. For the tests to be valid, the samples must be representative of the product. If the manufacturing process, which includes the materials, equipment, and processes, is controlled, then the test results may be valid. Many times, however, the manufacturing process is not controlled, which can lead to significant variability in quality, and erroneous reliability predictions.

Prior to commencing reliability studies, the manufacturing process must be controlled so that the test samples are representative of product. Ongoing control is required of the manufacturing process, to ensure that future products comply with earlier reliability tests.

Conductor Quality

Circuit boards are typically manufactured on large panels. A common size widely used in the industry is 18" wide by 24" long. Depending upon the manufacturing process, conductor widths, which are designed to be the same size, can vary significantly over the surface of panels, from side-to-side on panels, from panel-to-panel, and from lot-to-lot. The following table illustrates the variation measured over ten panels on 6-mil-pitch (3-mil lines and 3-mil spaces) technology, manufactured together as one set.

	Conductor Width	Resulting Space Width
Target Width	3.00	3.00
Minimum	2.43	3.57
Mean	3.12	2.88
Maximum	3.84	2.16
Standard Deviation	0.25	-

Table 1: Conductor and Space Variation

In this example, the designed space width is 3.0 mils. Because the process lacked proper control, the spaces varied from 2.16 mils to 3.57 mils. Deviation over the surfaces of the panels, from side-to-side on the panels, and from panel-to-panel, contributed to conductor and space width variability. Lot-to-lot deviation will impart additional variability on conductor and space width manufactured by the same process.

The degree of variability in space width will affect the reliability results, depending upon the placement of the test coupons on the panel area, and the particular panel(s) used in the tests. If, by chance, all reliability coupons used in the analysis were selected from areas with widths within ± 1σ about the mean, then the minimum space evaluated would be 2.63 mils. If all of the test coupons exceed the minimum time-to-failure for acceptable reliability, one would conclude that the process meets reliability specifications. However, the minimum clearance of 2.16 mils was evaluated in this example. Product that is manufactured with this clearance may, or may not meet the reliability requirements. Hence, the materials, equipment, and processes should be optimized and controlled prior to final reliability tests. Once a process is deemed acceptable, controls should be maintained to ensure that products continue to meet reliability expectations.

Microvias

Sequential-build technologies have been developed, and will continue to be developed to address the interconnection

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requirements of the future. Many alternatives have been pursued to produce microvias including: photodefinition, laser ablation, plasma etch, and mechanical drill. Each alternative requires tradeoffs in material properties to be compatible with processing equipment and end-point requirements. Reinforced dielectrics, for example, are generally not compatible with most methods to form microvias. Prerequisites for photodefined materials require that a pinhole-free dielectric conform to the previous layer with adequate adhesion, via holes are cleanly defined and developed to the layer below, and copper may be plated in the vias and patterned on the surface, all while achieving acceptable reliability.

The materials, equipment, and processes that are used to create microvias should create them consistently and uniformly over the surface of the panels, from side-to-side, from panel-to-panel, and from lot-to-lot. Not unlike conductors, variations in microvia may be characterized by precision resistance measurements. A tightly-controlled distribution of readings indicates that the process is well- controlled, while broader distributions, or ones with tails extending well beyond three standard deviations indicate a lack of process control.

The Via Net Resistance is plotted versus Design Number in the Figure 1. In this case, the through-hole vias were formed by conventional mechanical drilling. The distributions are displayed as notched box plots, with 50 percent of the data contained within the boxes, and nearly all of the data falling within the bars at the ends of each box. Individual data points that extend beyond the bars are plotted as dots, and termed "outside values." These outside values show considerable variability in the manufacturing process.

Reliability studies on test coupons manufactured by this process could provide erroneous results. If coupons were selected from within the bulk of the data and passed reliability tests, one may assume that the materials, equipment, and processes used in their manufacture are acceptable. Since the coupons corresponding to the outside values were not included in the evaluation, their impact on reliability will not be known.

On the other hand, if coupons corresponding to the outside values were included in the reliability study, and they failed, one may conclude that the process is not reliable. While this conclusion makes sense, perhaps all that is needed is an understanding of the factors contributing to the variability; once controlled - the process is reliable.

Thus, it is important to quantify the manufacturing process in terms of uniformity to ensure that meaningful results are obtained prior to large-scale reliability tests.

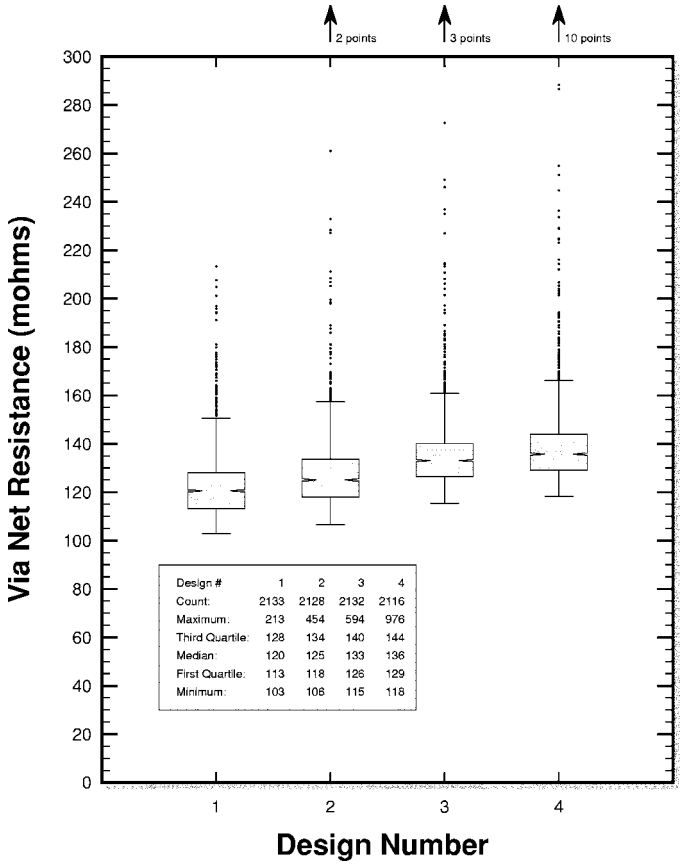

Figure 1: Via Net Resistance by Design Number

Summary

New technologies that are being developed and introduced to manufacture PWBs, require reliability testing to ensure high-quality, long-lasting, reliable products. The opportunity for failure increases as feature sizes decrease. Narrower lines and spaces, smaller holes, and thinner dielectric layers all pose potential threats to reliability. New materials, which are developed for sequential-build technologies, are formulated with tradeoffs in function, processing, and reliability.

Reliability studies are expensive and time-consuming. Studies performed on processes that are not controlled can lead to erroneous conclusions and costly mistakes. Before beginning reliability tests, the materials, equipment, and processes under investigation should be optimized in terms of uniformity to minimize variability over the surface of panels, from side-to-side on panels, from panel-to-panel, and from lot-to-lot. After the process has been characterized and controlled, reliability tests will provide data that is representative of the process intended to manufacture product. The manufacturing process should continually be controlled to minimize variability, and ensure that product continues to meet reliability expectations.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume III • Issue 12**

QUANTITATIVE MEASURES OF QUALITY

Introduction

The manufacture of quality products relies on processes that are reproducible and controlled. Many times, holding process parameters such as speed, temperature, concentration, and time to established values will lead to the desired quality in the finished product. With the formation of conductors on PCBs, opportunities for variation emerge from a multitude of sources. Simply turning each "knob" to an established setting will not provide the necessary control on conductor width and height, nor will it provide insight to improve quality.

Measurements of conductor width and height can provide data that quantify variation, identify sources of dispersion, and provide solutions to improve quality. Changes in process parameters, however, should not be based on a "handful" of measurements. Electrical resistance measurements from conductors provide an excellent source of data to characterize conductor width and height variation. A ten-panel set, for example, provides over 28,000 measurements on which to base decisions.

With so many data points to decipher, statistical measures are necessary to condense the data so that process changes may be made with confidence. The capability potential index, C_p, and the capability performance index, C_{pk}, are two indices that provide insight into the precision and accuracy of the features relative to the target. A third measure, the coefficient of variation, provides the relative variation of the feature with respect to the mean.

Capability Potential Index

The capability potential index C_p, is defined as the difference between the upper and lower specification limits, divided by six standard deviations. This measure compares the specification limits to the spread in the data.

$$C_p = \frac{USL - LSL}{6\sigma}$$

where

USL = upper specification limit

LSL = lower specification limit

σ = standard deviation

Capability Performance Index

The capability performance index C_{pk} compares the mean with the specification limits by the following equation:

$$C_{pk} = \text{minimum}\left\{\frac{USL - \mu}{3\sigma}, \frac{\mu - LSL}{3\sigma}\right\}$$

where

μ = mean

If the mean is centered within the specification limits, then C_{pk} will be equal to C_p; otherwise, it is less than C_p, and $C_{pk} \le C_p$.

Coefficient of Variation

The coefficient of variation (CoV), which is sometimes called the relative standard deviation, normalizes the standard deviation to the mean. The coefficient of variation, expressed in percentage, is defined by the following equation:

$$\text{CoV} = 100\ \sigma\ /\ \mu$$

Example Data

The following table shows results from a set of ten conductor panels that were manufactured by an outerlayer process. The design had 3-, 4-, 5-, and 6-mil wide conductors. Target widths for the finished conductors were 1.25 mils narrower than corresponding artwork features. The ten panels provided a total of 7040 conductors for each of the four sizes. The "count" in the table reflects the number of "good" conductors; those that were not open, and not shorted to a neighboring conductor. The specification limits for the control indices were ± 20 percent about the target.

While the mean conductor widths for each size were within 0.15 mils of the target, the large standard deviations contributed to small values for capability potential and capability performance indices. The coefficient of variation shows that as features become narrower, tighter control is required for comparable quality.

The last row in the table shows the statistics for the copper thickness. In this case, the target was missed by 0.31 mils, which contributed to the very low values for C_p and C_{pk}.

Target	Count	Mean	Sigma	CoV	Cp	Cpk
1.75	6684	1.87	0.330	17.61	0.35	0.23
2.75	6684	2.90	0.334	11.54	0.55	0.40
3.75	6683	3.88	0.331	8.53	0.75	0.62
4.75	6685	4.88	0.331	6.78	0.96	0.83
1.80	6685	2.11	0.168	7.97	0.71	0.10

Summary

Electrical resistance measurements provide excellent data to characterize manufacturing processes. With the abundance of available data, statistical measures such as capability potential, capability performance, and coefficient of variation provide a concise summary of the results that may be used to compare and improve processes. Once a benchmark has been established, the details of the data may be examined to uncover sources of variation, and used to modify the process and improve product quality.

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Between The Conductors

Conductor Analysis Technologies, Inc. **Volume IV • Issue 7**

MINIATURIZATION

Electronic products of tomorrow will become smaller, faster, more powerful, and less expensive than the products that are available today. The challenges that have been met by electronics manufacturers over the past years will not only continue, they will be more difficult. Future designs will require lower voltages, higher frequency, shorter signal paths, greater impedance control, and greater EMI control. The printed circuit boards of the future will require narrower conductors and spaces, smaller holes, and tighter registration capability to keep pace. This issue will examine how miniaturization affects PWB manufacturers' capability and quality.

Trends

Manufacturers of circuit boards have invested in materials, equipment, and processes to accommodate one or more "standard" panel sizes on which to build the circuits. One size, commonly used in the industry is 18" by 24". Some manufacturers use larger panels, which measure 24" by 30" and 24" by 36", to increase throughput and accommodate larger circuit boards. One or more circuits are placed on the panel area to maximize panel utilization and reduce scrap.

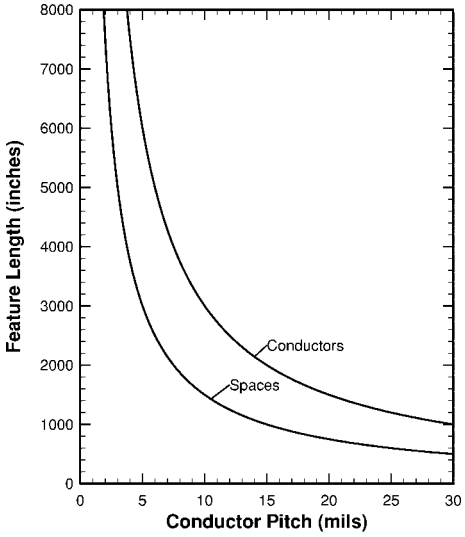

Figure 1. Feature Length vs. Conductor Pitch

Figure 1 is a graph that estimates feature length per layer versus conductor pitch (linewidth plus spacewidth). The curves shown in the figure are based upon 18" by 24" panels with an active area of 300 square inches, 10 percent utilization of active area, and a space-to-conductor length ratio of 50 percent. Technological advancements over the past 25 years have allowed conductor pitches to decrease from approximately 30 mils to below 10 mils. The benefits of increased interconnection density afforded by decreased conductor pitch are illustrated in Figure 1. Conductor and space length increase dramatically with narrower conductors and spaces.

While the trends in conductor pitch illustrated here are important, they do not tell the full story. Other factors that impact circuit density are hole diameter, land diameter, and registration. Additional wiring tracks may be placed between pads by decreasing the land diameter, providing increased interconnection density. Suppose improvements in drilling and registration changed the utilization of the active area from 10 percent to 20 percent, as shown in Figure 1 and Figure 2, respectively. These improvements in capability shift the curves toward greater conductor and space length for the same conductor pitch.

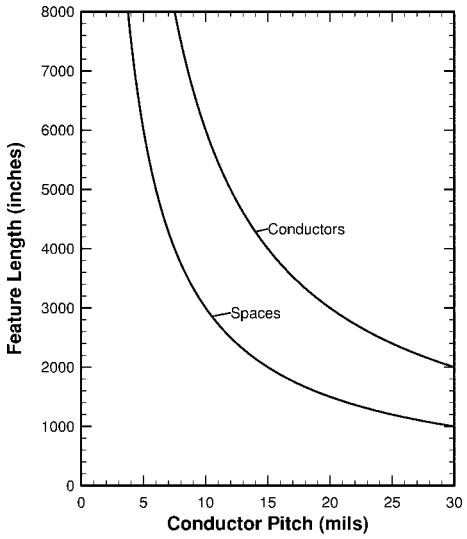

Figure 2. Feature Length vs. Conductor Pitch

New technologies that provide microvia capability further increase circuit density. Through-holes and through-vias block routing on every metallization layer in the multilayer structure. Microvias are used to interconnect some of the layers in the structure, and free routing tracks on the other layers. Further, microvias and their associated lands are smaller than the holes and lands required for through-vias, thus, allowing for increased density.

Yield Issues

The trends established over the past 25 years are clear, and will continue into the foreseeable future. Advancements in miniaturization allow greater conductor and space length, and greater numbers of holes to be placed within the same area. These narrower features and smaller holes are not only more difficult to manufacture, but because of the increased lengths and counts, have to be manufactured at lower defect levels than before to maintain the same yields. To illustrate this dilemma, examine the curves shown in Figure 3. Feature yield is plotted versus feature length for 10, 20, 40, 80, 160, 320, and 640 defects per million inches of feature. Clearly, for a given defect density, yield drops off with increased feature length.

Suppose a manufacturer currently builds circuit boards with 5-mil lines and spaces at a defect level of 80 defects per million inches of conductor or space. From Figure 1, the conductor length at a pitch of 10 is 3000 inches and the space length is

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1500 inches. Referring to Figure 3 for 80 defects per million inches, conductor yield is estimated at 78 percent and space yield at 88 percent for a combined yield of 69 percent.

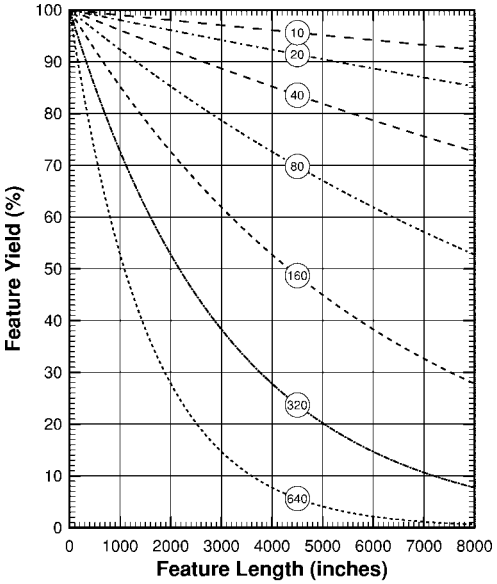

Figure 3. Feature Yield vs. Feature Length

The manufacturer plans to manufacture 3-mil lines and spaces on some new designs in the near future. From Figure 1, the new designs will have 5000 inches of 3-mil conductor and 2500 inches of 3-mil spaces per layer. If the manufacturer maintains the same defect levels, conductor yield is estimated at 67 percent and space yield at 82 percent for a combined yield of 55 percent. However, because the features are smaller and more difficult to manufacturer, defect levels will probably increase, perhaps to 160 defects per million inches of feature. If this were true, Figure 3 indicates conductor yield at 45 percent and space yield at 67 percent for a combined yield of 30 percent. To bring the yield levels up to those of the 5-mil lines and spaces, defect density must drop from 160 to approximately 50 defects per million inches of feature, better than the current capability for larger features.

Similar arguments hold for holes. The hole-formation and metallization processes depend upon the hole diameter, aspect ratio, and whether the hole extends through the board or is blind. For a given technology, smaller holes offer increased interconnection density, and are generally more difficult to form and metallize than larger ones. Thus, when moving to smaller holes, defect levels must improve to maintain equivalent yields.

Uniformity Issues

Conductor width and height uniformity is influenced by many factors. The size of the panel on which the circuit boards are manufactured is the starting point. Uniformity generally degrades with increased panel area. The interaction between the materials, equipment, and processes used to form the features is influenced by position on the panel surface. Additional variation occurs from side-to-side on a panel, from panel-to-panel, and from lot-to-lot. Major process steps that may contribute to variation include imaging, developing, etching, and plating.

The temporal and spatial effects that contribute to conductor width and height variation have had a relatively minor impact on large features. Conductor width standard deviation, measured over a set of ten 18" by 24" panels, typically varies between 0.1 mils and 0.4 mils, depending upon the process. The equivalent relative variation imposed on 8-mil wide conductors is 1.25 to 5.0 percent. When applied to a 3-mil wide conductor, the relative variation becomes 3.3 to 13.3 percent. If the conductor widths are normally distributed, ± 3 standard deviations encompass 99 percent of the data. Thus, in the worst case, the widths for the 3-mil wide conductor would range from 1.8 mils to 4.2 mils.

As features become smaller, hitting the target width becomes more difficult. In a print-and-etch process, for example, finished conductor widths are often narrower than the artwork feature width. Some manufacturers “grow” the artwork width to account for conductor width loss during the process. For 3-mil finished lines and spaces, a manufacturer may create artwork with 4-mil wide lines and 2-mil wide spaces. Problems begin when attempting to image, develop, and etch this 2-mil space uniformly over the area of the panel surfaces. If the photoresist is one-mil thick, the developed image has an aspect ratio of 0.5. During the etching step, the aspect ratio increases to 0.85 for half-ounce copper and 1.2 for one-ounce copper, leading to potential degradation in both yield and uniformity.

Keys to Success

Established trends in the electronics industry are expected to continue, requiring smaller features sizes on future printed circuit boards. As feature sizes become smaller, they are more difficult to form. Due to the greater lengths of conductors and spaces, and numbers of vias that reside within a constant area, defect densities must improve to maintain current yields. Further, conductor width and height uniformity must improve to maintain the same relative variation.

What are the keys to success? One of the keys is increased research and development by manufacturers and suppliers to develop new materials, equipment, and processes for fine line, small hole printed circuit boards. Aggressive long-term goals should be developed to provide technology beyond that which is expected within the next five years. Developers should use scientific methods incorporating experimental designs to measure and understand their process, so that calculated and quantifiable improvements are implemented.

Collaborative efforts among suppliers and manufacturers or between government and industry can lead to developments that would otherwise be overlooked. Shared resources allow companies to leverage their commitment, which benefits the participants and the industry. Advancements are inevitable, but the paths we take to achieve them can have a major impact on their success.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume IV • Issue 8**

INVESTIGATING PROCESS CAPABILITY - PRECLEAN

The materials, equipment, and processes that are used in the manufacture of printed circuit boards affect the quality of the finished product. Moreover, the absence of quality leads to increased pressure for testing and inspection, increased rework and rejects, lower yields, non-conformance, and higher costs. Defects uncovered at the end of the process may have their seeds early, midway, or late in manufacture. Identifying their source becomes a difficult task at times, perhaps because of the endless opportunities along the manufacturing process for problems to occur.

To improve capability and quality, each of the major process steps are discussed. Sources of defects and non-conformance are revealed, and techniques are suggested to uncover possible causes. This column concentrates on the preclean process, while subsequent columns will investigate photoresist application, imaging, developing, etching, drilling, and plating. The understanding gained by partitioning the manufacturing process, and investigating and improving each sub-process can lead to lasting, measurable improvements to capability and quality.

Preclean Process

The purpose of the preclean operation is to remove foreign substances from the substrate, leaving behind a clean copper surface. Some of the contaminates that are frequently found on panels include oils and grease, oxides, epoxy spots, glass fibers, and anti-tarnishing treatments containing chromium and zinc. Further, the preclean step is frequently called upon to roughen the copper surface, providing mechanical adhesion between the copper surface and the subsequently applied photoresist material.

The preclean process has been implemented in a variety of forms, depending upon its requirements. Chemical cleaning agents such as soaps, surfactants, and solvents are helpful in removing oils, grease, and foreign particulate contaminates. Mechanical scrub, or slurry of pumice or aluminum oxide is sometimes used to provide an additional margin, and to roughen the surface. As an alternative to mechanical cleaning techniques, a mild etchant may be used to roughen the copper surface by the differential attach of the crystalline structure. A mild acidic solution followed by a thorough rinse is often used to remove any oxides remaining after earlier preclean steps.

Issues

An inadequate or uncontrolled preclean process can lead to defects in the finished printed circuit board. These defects manifest themselves in two fashions: copper remaining on the finished circuit board where it was intended to be removed, and copper removed from the finished circuit board where it was intended to remain. There are many possible causes of these defects. Adhesion failure between the photoresist and copper can lead to "opens" and "near-opens" in a print-and-etch process, for example. While adhesion failure could be caused by downstream processes such as lamination or material flaws in the resist itself, remaining surface contaminates or inadequate surface roughening after preclean are likely candidates. In the same print-and-etch process, epoxy spots or anti-tarnish coatings remaining after preclean can delay or prevent copper etching, and result in "shorts" or "near-shorts" in the finished printed circuit board.

Contaminates Affecting Etching

The first test can establish the presence of contaminates on innerlayer cores that prevent etching, such as epoxy spots or anti-tarnish coatings. Process a set of innerlayer cores through the normal preclean operation, and then through the etcher. Since photoresist is not applied to these cores, all of the copper should be removed after etching. Inspect each core on a light table for the presence of copper. The back-lighting provided by the light table will allow the remaining copper to be visible to the unaided eye. Using this technique, a comparison between pre-cleaned cores and those skipping the preclean process may reveal the effectiveness of the preclean process. If copper spots remain after the preclean process, examine them with the aid of a microscope. If the remaining copper thickness is substantial, etching was either delayed or prohibited, indicating the presence of surface contamination.

Conditions Affecting Adhesion

Either surface contaminates or inadequate surface roughness can adversely affect the adhesion between the photoresist and copper. In the next test, a fine-line multi-pitch test pattern is used to quantify defects and copper removal as a function of preclean treatments. Fifteen innerlayer cores are randomly selected from the same supplier's lot, and marked 1 through 15. The panels are assigned different numbers of preclean cycles according to the following table. After the preclean process, these panels are processed sequentially in numerical order from 1 through 15. They are laminated with photoresist, imaged with the multi-pitch test pattern, developed, etched and stripped.

Panel Numbers	Number Of Preclean Cycles
1,6,11	0
2,7,12	1
3,8,13	2
4,9,14	3
5,10,15	4

Analysis of the electrical test data from these panels provides three response variables: number of "opens", number of "shorts", and copper thickness removal. If the results from this test indicate that the nominal preclean process is inadequate, an experiment designed around pertinent variables may be conducted using the same test pattern and response variables. Results from designed experiments provide the data for process engineers to justify process changes, and improve capability and quality.

Each process step in the manufacture of printed circuit boards can be the source of defects. The simple tests described here can help to identify potential problems, and provide techniques to improve the preclean process.

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Between The Conductors

Conductor Analysis Technologies, Inc. **Volume IV • Issue 9**

INVESTIGATING PROCESS CAPABILITY – PHOTORESIST

Printed circuit manufacturing involves a myriad of process steps acting sequentially on the "work piece" to add value (and cost) along the way. The materials, equipment, and processes acting on the "work piece" impart a signature, sometimes acceptable and sometimes harmful, that carries through to subsequent steps. Identifying the sources of aberration can provide process engineers with information necessary to correct problems, extend capability, and improve quality.

Covered in the last column, the preclean process was the first of many process steps to be discussed, which affect the level of technology a manufacturer will accept and the quality of the printed circuits manufactured. The photoresist and its application to the copper surface is the next step to be examined, while subsequent steps such as imaging, developing, etching, drilling, and plating will be discussed in future columns.

Photoresists

The photoresist provides an intermediate image between the artwork and the conductive metal pattern formed on the substrate surface. The quality of the finished conductive pattern depends upon the quality of the imaged and developed pattern formed in the photoresist, and the ability of the exposed and cross-linked resist to maintain adhesion during developing, plating, and/or etching.

Thin dry-film and liquid photoresists are often used for print-and-etch processes, while thicker resists are usually required for pattern-plating (print, plate-and-etch) to prevent the copper from depositing on the top surface of the photoresist. In both cases, the resist must conform and adhere to the pre-cleaned metal surface. Thin resists can extend fine-line resolution by providing improved sidewall definition and minimized aspect ratio for developing and etching. Some liquid resists have been designed for 0.2 to 0.3-mil thick films, while the thinnest dry-film resists are generally limited in thickness to about 1.0 mil. However, as dry-film resists become thinner, their ability to conform to the metal surface may decrease, and their susceptibility to pinholes may increase.

Sources of Defects

There are many opportunities for defects to occur in the finished copper pattern, which have their seeds in the photoresist material or the resist application process. Dust particles, resist flakes, hair, fibers, and other contaminates, which are laminated between the resist and the copper surface in a dry-film process, can cause loss of adhesion and non-conformance between the resist and the metal surface. Similar problems can occur if a liquid resist is applied to a metal surface having these contaminates, or if contaminates are in the liquid resist and applied with the resist.

Contaminates that fall on the resist surface after the resist application step must be removed prior to the imaging process, or they will produce defects, especially with the high-resolution photoresists available today.

Defects within the resist such as gel particles or pinholes, and fillers in the polyester that can scatter the UV radiation may cause defects to a lesser degree. Contaminates, non-conformance, and adhesion loss are the major sources of defects having their seeds in the resist application process.

Photoresist Application

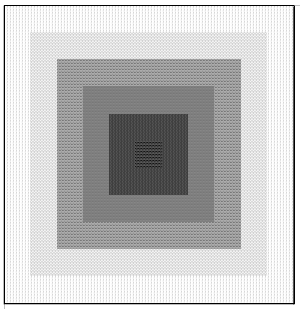
Dry-film photoresists are applied to the copper surface by controlling the temperature, pressure, and speed of the rollers in the dry-film laminator. Adequate adhesion of the resist to the copper usually results when the resist is applied to a "clean" copper surface at the correct temperature, pressure, and speed. Some dry-film resists are formulated for "wet-lamination," a process that adds water to the resist during lamination to lower viscosity and improve conformance between the resist and the copper surface.

Liquid photoresists are designed for many application methods, including electrodeposition, roller-coating, curtain-coating, and spray. Each method requires careful control of the resist chemistry and associated processing steps to assure pinhole-free coatings with adequate adhesion.

Regardless of the method of application, all photoresist processes require a cleanroom environment, especially for the high-resolution resists available today.

A Simple Test

Loss of adhesion between the photoresist and the copper surface is one factor that contributes to defects and conductor width variation. A test to study photoresist adhesion uses an array of small dots, which are imaged, developed, and inspected. The pattern consists of one-inch squares, replicated over the entire area of the panel. Each square contains multiple dot sizes, with the smallest at the center and largest at the perimeter. The dot pattern at the left is a schematic with six dot sizes per square inch, indicated by the level of shading. The size of the individual dots within each region depends upon the photoresist and process under investigation. Start with the smallest dots at three-to-five mils in width, with spacing comparable to width. Initially, increase each successive size by one mil. Examine the imaged and developed patterns for missing dots and undercut. Expect some dots to lift off during developing, but be careful that the dots are not too small, which could cause havoc in the developer or the following rinse should they all flake off.



Dot Pattern

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After inspection, the patterns can be etched to ascertain the physical and chemical impact of etching on adhesion.

Summary

The photoresist plays a significant role in the transfer of the image from artwork to copper. Aside from the defects caused by contaminates, loss of adhesion between the photoresist and copper may be the largest source of defects stemming from the photoresist application process.

A simple test using a pattern of dots can help to evaluate adhesion between the resist and copper, and to optimize processing parameters for the best adhesion. Variation in adhesion that is spatially-dependent will become evident with the patterns of dots remaining after this test. After development and inspection, the dot patterns can be etched to determine the impact of etching on adhesion.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume IV • Issue 10**

INVESTIGATING PROCESS CAPABILITY – IMAGING

In previous columns, the preclean and photoresist application processes were discussed. In this column, a study of the imaging process reveals sources of defects and non-uniformity, and offers courses of action to improve quality and capability. Future columns will be devoted to subsequent steps in the process, such as developing, etching, drilling, and plating.

Imaging Systems

Imaging systems may be characterized as contact printers or non-contact printers. In contact printing processes, the artwork is brought into "hard contact" with the photoresist by applying a vacuum between the two, or "soft contact," where mechanical forces hold the two together but a vacuum is not created. Non-collimated illumination sources generally require hard contact between the artwork and resist. Highly collimated sources are generally required for soft-contact imaging, but they may be used in both hard- and soft-contact systems.

Non-contact printers include proximity printers, projection printers, and laser direct imaging systems. Proximity printers are often used for wet or tacky photoresists to maintain approximately 10- to 20-mils of separation between the photoresist and artwork. This technology requires a highly collimated illumination source to prevent the image from blurring. In projection printers, a lens is placed between the artwork and the photoresist, keeping the artwork a great distance from the resist. Laser direct imaging systems do not use artwork. The CAD data are used to apply the laser beam to the photoresist, creating the image directly.

System Parameters

There are many factors that influence the quality of the image formed in the photoresist by the imaging system. Illumination intensity, wavelength(s), exposure dose, uniformity, and collimation play important roles and provide trade-offs.

The spectral output from the illumination source must include ample energy at wavelengths that are absorbed by the photoinitiator to complete the cross-linking process. Most UV-sensitive photoresists have photoinitiators that are tailored to absorb the 365 nm peak found in mercury and mercury/xenon arc lamps. The presence of oxygen, found within the photoresist or in close proximity to the photoresist, inhibits the reaction to cross-link the polymer. The UV source must supply sufficient energy (governed by intensity) at the appropriate wavelength to create free radicals at a rate faster than the available oxygen quenches them, in order for the process to proceed. When collimation is necessary, as in soft-contact, proximity, or off-contact printing, the additional required optics reduce the intensity and increase the exposure time for an equivalent exposure dose.

Environment

The printing environment must be carefully controlled and maintained for best results. Cleanliness is of utmost importance. A well-maintained laminar flow clean room with hepa filters is necessary, but not sufficient for success. The operators, maintenance, and engineering personnel must wear appropriate clean room garb, and follow clean room procedures to minimize defects caused by dust, fibers, hair, and other particulate contaminates. Sources of contamination, which are carried in on the boards being processed, include glass fibers, copper flakes, and epoxy chips, while hair and flakes of skin come from the people working in the clean room.

Yellow lights are usually required to prevent unintentional exposure of the UV-sensitive photoresist, while tight temperature and humidity controls are required to minimize film and substrate distortion that lead to registration errors.

Sources of Defects

Most defects that occur from the imaging process are a result of exposing areas of resist that were to be unexposed, or not exposing areas that were intended to be exposed. The artwork holds the image to be transferred to the photoresist. Defects in the artwork, where transparent and opaque regions are transposed, will be reproduced faithfully to the degree that they can be resolved, leading to "repeating" defects in the photoresist.

Aside from defective artwork, contaminates can effectively "transpose" regions of the artwork by blocking radiation in transparent areas, or scattering radiation to resist under opaque areas. Defects caused by contamination may manifest themselves as "repeating" if the position of the contamination is fixed, or "random" if the contaminates move about from print to print. Hair and fibers often lead to "events" that affect many features in close proximity to one another.

When artwork is held off-contact by contaminates during contact printing processes, UV radiation will scatter to resist areas under the opaque regions of the artwork, especially with non-collimated sources. Areas of off-contact can result from hair, fibers, and particles trapped between the artwork and resist, or between the resist and copper. Thus, a well-maintained clean room environment is essential to reduce the impact of contaminates on quality.

Feature widths that are intended to be uniform can vary over the surface of the panel if the exposure intensity is non-uniform. Further, inadequate vacuum in hard-contact printers can lead to soft-contact or off-contact areas, which cause feature widths to vary. Defects arising from variations in exposure intensity and inadequate vacuum are often found systematically in the same area(s) of each panel.

Printing Process Check List

The following tasks can help uncover and eliminate defects

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and non-uniformity created during the printing process.

- Check the spectral output of the lamp at the exposure plane. The relative intensity of peak wavelengths often changes as the lamp ages. The coatings on optical components also age with time, and can degrade performance. Be sure the peak wavelength (usually 365 nm) that the photoinitiator absorbs is strong.
- In collimated printers, check the collimation angle over the exposure area to ascertain that it is uniform and within specification.
- Measure the illumination intensity over the exposure area, and adjust optics as necessary for best uniformity (without sacrificing collimation when collimation is required).
- Check the printing frame for damaged mylar or glass, and replace damaged components as required.
- In vacuum printers, look for the presence of Newton rings to confirm hard contact. If some areas are void of Newton rings or the time to achieve them is prolonged, check that the vacuum source is within specification and check for possible leaks in other areas.
- Check clean room procedures. Be sure that all shop, maintenance, and engineering personnel faithfully follow established procedures.
- Check incoming panels for the presence of contaminates such as glass fibers, copper flakes, and epoxy chips. If necessary, modify the preclean process to eliminate contamination.

Summary

The PWB imaging process is supersensitive to cleanliness, particularly when manufacturing high-density, fine-line product. Any defects that begin in the imaging process will be carried through subsequent steps, and materialize in the finished conductive patterns. "Shorts" between conductors and "opens" within conductors lower process yield and increase manufacturing cost, while "near-shorts" and "near-opens" lead to reliability issues and potential failure in the finished product.

While cleanliness is imperative, the imaging equipment must be properly maintained to minimize variation in feature width over the panel surface area, from side-to-side on panels, and from panel-to-panel. Periodic checks and measures can help ensure that the equipment is operating at peak performance and the product manufactured is the highest possible quality.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume IV • Issue 11**

INVESTIGATING PROCESS CAPABILITY – DEVELOPING

In previous columns, capability was investigated for the preclean, photoresist application, and imaging processes. This column discusses the sources of defects and non-uniformity in the photoresist developing process. A simple test used to reveal treatment uniformity is introduced.

Future columns will be devoted to subsequent steps in the process, such as etching, drilling, and plating.

The Function of the Developing Process

The printing process for negative acting, UV-sensitive photoresists starts with a uniformly "uncross-linked" polymer film that is converted to regions of "cross-linked" polymer by exposure to UV radiation. Positive-acting UV-sensitive photoresists begin with a uniformly "cross-linked" polymer film that is converted to regions of "uncross-linked" polymer by breaking bonds in areas exposed to UV radiation. In both cases, the "uncross-linked" regions are soluble in the developer, while the "cross-linked" regions are insoluble. However, the imaged photoresist is not simply divided into "cured" and "uncured" regions, but exhibits a transition at the edges of the desired features where the degree of cross-linking varies from "cured" to "uncured". Thus, depending upon the characteristics of this transition region, the developed features will grow with extended development conditions and expose additional copper for subsequent plating and/or etching.

On a macroscopic scale, the developer should remove "uncured" photoresist uniformly over the surface of the panel, from side-to-side on panels, and from panel-to-panel, leaving a clean copper surface in these areas and the "cured" photoresist intact. The developer "breakpoint" is often used to establish the transport speed at which to process the panels. The "breakpoint," expressed in percent, is the point in the developer chamber that all "uncured" resist is removed from the copper surface. The "breakpoint" may be recommended by the photoresist manufacturer or determined experimentally, and is commonly between 40-60 percent.

On a microscopic scale, uniform and straight photoresist sidewalls with minimal "foot" are desirable. As feature sizes become smaller, the aspect ratio of the fully developed region (for a given resist thickness) becomes larger, and mass transport across the boundary layer becomes increasingly important. Dissolved photoresist must be carried to the bulk solution, while fresh developer must be supplied to the photoresist surface to complete the process.

The rinse following the developer halts the developing process, removing developer solution and dissolved resist from the surfaces of the panels.

Developing Equipment

Commercially available conveyorized equipment, used by PCB manufacturers to develop photoresist, transports the panels either horizontally or vertically. While each type is capable of developing the resist, the signature left on the product may be significantly different, especially when manufacturing narrower lines and spaces. The differences stem from the interaction of gravitational forces with the fluid dynamics of the developer solution.

Horizontal transport systems must contend with the puddling phenomena on the top side of the panels, which often creates non-uniform treatment over the surface. As developer solution is sprayed on the top surface, flow patterns emanate from the center of the panel to the perimeter. The puddle is usually thickest at the middle where the surface velocity is smallest, and thins toward the perimeter with increased surface velocity. These macroscopic conditions cause differences on the microscopic level by affecting the thickness of the boundary layer, as well as the transport of dissolved photoresist and fresh developer solution across it. Because the flow conditions are so different from the bottom side of the panels, a top-to-bottom-side treatment difference is common as well.

In vertical developer systems, panel side-to-side differences are usually small because both sides are symmetric with respect to the gravitational forces that interact with the developer solution fluid dynamics. However, treatment uniformity may suffer over the panel surface because of the acceleration and thickness variation of the "sheet" of fluid as it falls over the panel surface from the top edge to bottom edge. Further, significant treatment variation may occur from laminar, transition, and turbulent flow patterns that are caused by the orientation of the features – either parallel or perpendicular to the surface velocity vector of the developer solution.

The fundamental differences between horizontal and vertical developer systems aside, equipment manufacturers offer features that are designed to address the issues of treatment uniformity. Spray nozzle design, placement, and motion, along with spray pressure and volumetric flow can influence treatment uniformity. Other features commonly available on most developers include speed control, temperature control, filtration, "feed-and-bleed", and thin-core transport.

The Developing Solution

The developer chemistry depends upon the photoresist. For aqueous-developable photoresists commonly used in the industry, an alkaline solution of approximately one percent by weight of sodium carbonate or potassium carbonate is often used. Anti-foam agents may be added to the developer to prevent foaming. In some cases, a "batch" of new chemistry may be used to the end of its useful life and then discarded. More commonly, a "feed-and-bleed" process is used, which circulates the developer solution through filters, discards a small volume, and adds fresh solution to maintain a constant pH and level of dissolved resist.

Sources of Defects

The developing process cannot fix (nor should it be expected

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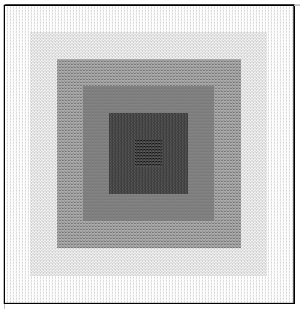
to fix) upstream problems resulting from raw materials, preclean, resist application, or imaging. The resulting developed image can be no better than that which is supplied in the photoresist by the previous steps. However, the developing process can degrade the image, and even cause defects that will be carried through to the finished pattern that is plated and/or etched in copper.

Mechanical damage to the photoresist, caused by operator mishandling or problems with the conveyorized transport system, is a potential source of defects. Incomplete developing caused by blocked spray nozzles is a common source of defects. Variations in transport speed, developer temperature, concentration, pH, and resist loading can lead to defects as well. As features get smaller, treatment uniformity can play an increasingly important role in the quality of the finished circuits.

The rinse following the developing process stops the dissolution process, and removes developer solution from the panel surface. If this rinse becomes loaded with excessive amounts of dissolved resist, a film that prevents plating and/or etching may redeposit on the exposed copper surfaces, resulting in another source of defects.

A Simple Test for Treatment Uniformity

A pattern of small holes is used to investigate developer treatment uniformity. Similar to the pattern introduced to study photoresist adhesion, the pattern consists of one-inch square images that are replicated over the panel surface area.



Hole Pattern

Each one-inch square contains small square holes to be developed – the smaller the opening, the more difficult the task. Multiple hole sizes, with the smallest at the center and the largest at the perimeter, are included in the design to quantify local treatment capability. The pattern at the left is a schematic with six hole sizes per square inch, indicated by the level of shading. The size of the individual holes within each region depends upon the thickness of the photoresist. Select the largest opening size to ensure that most or all of these holes will be developed cleanly over the entire surface area of the panel. The smallest openings should be sized so that very few are successfully formed, while the intermediate sizes will show a range of performance, dependent upon the local conditions during development.

The pattern should be imaged on one side of a core clad with relatively thin (half-ounce or quarter-ounce) copper. Photoresist on the other side of the core should be unexposed (for negative-acting photoresist) to make certain that all copper on that side will be removed in the etching step. In horizontal processing equipment, develop some of these patterns facing up and others facing down, keeping track of leading edges so that the results can be correlated to the equipment. In vertical processing developers, process some panels facing left and others facing right, again keeping track of orientation to trace performance back to the equipment.

After developing, process the cores through the etcher at a slower-than-normal transport speed to provide ample opportunity for etching the copper from the small openings formed in the photoresist. After rinsing and drying, place each core on a light table to backlight the image formed by the pattern of squares. The patterns observed will reveal variations in treatment over the area of the panel surface.

Summary

The developing process combines electromechanical systems with chemical processes in the presence of gravitational forces, dissolving uncross-linked photoresist from the surfaces of panels while leaving cross-linked resist intact. The quality of the developed features depends upon the interaction of the developer with the photoresist, and the ability to transport fresh solution and dissolved resist across the boundary layer to and from the photoresist surface, respectively. Macroscopic conditions that influence the fluid dynamics of developer solution at the panel surface impact performance on a microscopic level, leading to non-uniform treatment over the surface of the panel. As feature sizes become narrower, treatment non-uniformity becomes increasingly important.

While the developing process cannot fix upstream problems, defects can begin in this process step. Mechanical damage to the photoresist and incomplete development are potential sources of defects that could have their seeds in the developing process.

A simple test to investigate developer treatment uniformity was introduced, which employs a pattern with a variety of sizes of tiny squares. A selection of one-inch square hole patterns is available on the WEB at http://biz.swcp.com/cat. The visual impact of completed panels inspected on a light table is helpful to identify and explain sources of non-uniformity.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume IV • Issue 12**

INVESTIGATING PROCESS CAPABILITY – ETCHING

It is difficult, if not impossible, to improve a process without sound data – the basis for making changes. The topic for the past four months has been "Investigating Process Capability." During that time, the preclean, photoresist application, imaging, and developing processes were examined for sources of defects and non-uniformity, and simple tests were presented to indicate deficiencies. This column continues with a glimpse at the etching process.

Future columns will discuss two remaining steps in the circuitization process – drilling and plating.

The Etching Process

The etching process transfers the image that was previously formed in the resist to the conductive layer, by removing (etching) unprotected copper and leaving protected copper intact. Copper dendrites, which provide mechanical adhesion between the foil and the substrate, may be rooted in the dielectric and must be removed as well.

The etching process is inherently isotropic, etching down and laterally at the same rate. The cross-section of features formed by isotropic etching usually show conductors that are narrower at the top than the bottom, with concave sides.

As feature sizes become smaller, anisotropic etching is desirable to minimize lateral attack and create straighter sidewalls, with the conductor width at the top nearly equal to that at the bottom. Some manufacturers have added "banking agents" to the etchant to produce anisotropic etching.

Both alkaline and acid chemistries are suitable for etching copper. Two of the most common etchant chemistries used by the PCB industry are ammoniacal etchant and cupric chloride etchant.

Etching Equipment

Most commercially available etching systems used by the PCB industry transport the panels on rollers horizontally through the equipment. Systems usually include one or more etching chambers, where the etchant is applied (usually sprayed) to the board surface, followed by cascading rinsing chambers. Transport speed, etchant temperature, nozzle type, and spray pressure adjustments are standard on most systems. Nozzle oscillation, thin-core transport, and automatic replenishment systems are available on most systems as well. At least one equipment supplier offers a delayed on/off spray option to improve leading-to-trailing edge treatment uniformity.

Equipment design along with available controls impact treatment uniformity. Similar to horizontal developers that were discussed in the last column, puddling is a major source of non-uniformity on the top side of panels processed through horizontal etchers. Treatment uniformity depends upon the transport of fresh etchant and byproducts across the boundary layer to and from the copper surface respectively, consistently over the area of the panel. The puddling phenomena causes the etchant to be thickest at the middle of the panel, where the velocity of the etchant is lowest, and thins toward the panel edges, where the velocity is highest. These macroscopic effects govern the etch rate on the microscopic level, creating non-uniform treatment over the surface of the panel.

Sources of Defects

Except for extreme uniformity problems or incorrect settings, most defects remaining after the etching step are latent, resulting from steps in previous processes. The etching process cannot fix (nor should it be expected to fix) problems stemming from preclean, resist application, imaging, and developing. The etchant will oxidize only the copper that is exposed to the etching solution.

Photoresist adhesion loss can lead to "opens" and "near opens" in a print-and-etch process (using a negative acting photoresist) or "shorts" and "near shorts" in a pattern plating process. Adhesion between the resist and the copper depends upon well controlled preclean and resist application steps. Oils, grease, and other organic compounds must be removed by the preclean process, which may be called upon to roughen the copper surface as well.

Particulate contaminates, such as dirt, dust, hair, epoxy chips, and glass fibers can cause a false image transfer from the artwork to the resist, and lead to defects. As the demand for narrower lines and spaces increases, higher resolution photoresists and imaging systems that inherently resolve smaller particles are required. Thus, the clean room environment must be well maintained to minimize the impact of particulate contaminates on yield.

Defects in the artwork or contaminates attached to the printing frame can cause "repeating defects" in the etched pattern.

Residues of resist in areas intended to be clear can result from inadequate developing (or the rinse following the developer), leading to defects in the etched pattern. An over-aggressive developer can cause the photoresist to lift, creating defects as well.

In some instances, mechanical damage to the resist or copper may occur from mishandling the panels, or from a malfunction in the conveyorized transport system.

Sources of Non-uniformity

In addition to the puddling phenomena mentioned earlier that occurs on the top side of panels, there are many other sources of etching non-uniformity. The etcher cannot be expected to improve upon the non-uniformity embedded in the image by previous process steps. For example, artwork off-contact areas during the imaging step can spread the image in the photoresist, while non-uniformities in the developer can distort the developed image.

Etching over the surface of a panel is dependent upon the diffusion of fresh etchant from the bulk solution to the copper surface and byproducts from the copper surface to the bulk

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solution across the boundary layer. This transport process is affected by the fluid thickness on the panel surface, the fluid velocity, and whether the flow is laminar or turbulent. Typical problems include variation from leading to trailing edge, preferential etching bias between horizontally- and vertically-orientated conductors, stripes caused by clogged nozzles or unbalanced spray manifolds, top-to-bottom difference due to unbalanced spray pressures, and shadowing due to transport rollers and thin material transport mechanisms.

Another possible source of variation is the nozzle oscillation rate relative to the transport speed. For systems with this option, the oscillation tends to push the puddle off the panel surface, and mixes the solution to improve the transport of fresh chemistry and byproducts across the boundary layer. If the oscillation rate is too high, the puddle will simply move back and forth without reducing the fluid thickness on the panel surface. Alternatively, if the oscillation rate is too low, some areas on the panel surface will see the thinning effects of the directional spray, while other areas will not.

Panel-to-panel variation due to etching chemistry or temperature change is another source of non-uniformity. Depending upon the feedback loop, systems with controls for automatic additions of chemicals can cause a cyclical variation in etch rate that will imprint a large variation on the desired width of features.

Methods to Measure Defect Density and Treatment Uniformity

Both optical and electrical methods have been used by manufacturers to characterize capability and quality. Optical methods, employing visual inspection, eye loops, microscopes, and automatic optical inspection equipment are especially useful in finding defects in product. Once the defect is discovered, the part may be repaired or scrapped. But because of design variations found in product, little information is available to establish the defect density of the process.

Cross-sections of features examined by microscope are often used to identify defects and measure feature sizes. The data gathered are from localized regions, at the position of the cross-section. To quantify treatment uniformity, measurements from hundreds or perhaps thousands of cross-sections are necessary, a practical limitation of this method.

Electrical measurements are used to test for "opens" and "shorts" in product, using low voltage continuity, and "near opens" and "near shorts" with a high voltage breakdown test. These tests are performed on product to ensure functionality, but do not provide data to calculate uniformity or defect density.

Conductor Analysis Technologies, Inc. has developed methods to characterize circuitization processes using specially designed test patterns, electrical test, and data analysis. Precision electrical resistance measurements from conductors on the test patterns are used to quantify defects, and calculate conductor width and conductor height. Statistical analysis of the data provides both defect density and uniformity information necessary to characterize and optimize etching equipment. With a spatial resolution of one-square-inch, a set of ten panels can provide over 28,000 measurements that may be used as the basis for defect density and uniformity calculations. These data portray the local variations and quantify total variation of the imaged, developed, and etched panels, which are characteristic of the process used in their manufacture.

Summary

The job of the etcher is to remove completely (etch) unprotected copper from the panel, and leave intact the copper protected by resist. If accomplished perfectly, the completed image will reflect the imperfections and variation from earlier process steps.

Most defects that remain after etching result from failure in earlier processes. Inadequate preclean, contaminates from resist application and exposure, under- or over-development, and poor rinsing after development are common sources of defects. However, improper etcher settings and extreme treatment non-uniformity can cause defects as well, especially when manufacturing high-density fine line product.

In practice, the etching process adds significant variation to the desired width of features. This variation is caused in part by inconsistent transport of fresh etchant and byproducts across the boundary layer to and from the copper surface, respectively. Additional variation occurs from changes in etchant chemical activity with temperature and time. Automatic controllers designed to maintain a constant level of chemical activity, in fact, maintain activity within limits that result in variations of feature width from panel-to-panel.

Precision electrical resistance measurements made from conductor nets on specialized test patterns provide the most comprehensive quantitative data to characterize and improve etcher performance. Without good data, engineers lack the information necessary to make the proper changes to improve etcher performance.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume V • Issue 1**

INVESTIGATING PROCESS CAPABILITY – DRILLING

Previous columns discussed the preclean, photoresist application, imaging, developing, and etching processes, with simple tests presented to investigate process capability. This column continues this objective with a discussion of the drilling process. Next month's column will complete the topic of *Investigating Process Capability* with a discussion of metallization.

The Drilling Process

The demand for circuit miniaturization has created the need for smaller holes and microvias, smaller lands, narrower lines and spaces, and tighter registration. To address the need for smaller holes, research and development programs have extended mechanical drilling capability, and created a host of alternative methods to form holes.

Along with alternative methods of forming holes, the drilling process is essential in the manufacture of printed circuit boards. The holes provide the path for subsequent metallization that interconnects conductive nets from layer to layer. The quality of the interconnection begins with the quality of the hole.

Holes may be characterized as two types: through-holes, which extend through the entire structure after they are formed, and blind holes, which have access from just one side of the structure. Through-holes may provide connection from one side of the structure to the other, or connect to one or more internal layers and bring the connection to the surfaces of the structure. The through-hole drilling process cuts through metal pads on internal layers (when present), and exposes a cylinder the diameter of the drill and the height of the internal metal layer for subsequent connection to the plated barrel of the hole. The drilling action often raises local temperatures above glass-transition, smearing dielectric onto the sidewalls of the hole, and coating both the freshly cut dielectric and metal cylindrical surfaces. Work hardening may change the properties of the metal, sometimes causing it to become brittle – leading to potential failures. To address these issues, de-smearing, etch-back, and mild copper etching steps are often employed to remove the drill smear, and to clean and roughen the copper surfaces intersecting the holes. Through-holes often have relatively high aspect ratios, made possible by advancements in drilling and metallization technologies.

Blind holes usually provide interconnection between an exposed layer (at the time of formation) and the surface of a metal pad on an internal layer. Blind via holes become buried or stacked vias when the hole-formation and metallization processes are repeated in a sequential-build approach. For reliable interconnections, blind via holes must extend to the pad on the internal layer, and the bottom of the via hole must reveal a clean copper surface that is free of dielectric residue and other contaminates. Blind via holes usually have a relatively low aspect ratio, if not for the hole formation process itself, then because of the dynamics of the metallization process.

Methods of Hole Formation

Mechanical drilling is the most common method of forming holes for interconnections in printed circuit boards. Drill diameters ranging between 0.059 and 0.010 inch are commonly used to provide through-hole interconnections in multilayer boards. Smaller diameter vias, perhaps as small as 0.006 inch, may be created by drilling through-holes in thin innerlayers, followed by metallization and patterning processes. When laminated into the multilayer structure, the holes in these innerlayers become buried vias.

Mechanical drilling may also create blind holes by a technique termed *controlled depth drilling*. In this case, the drill point must pierce the land(s) on the layer(s) to be connected. Hole diameters as small as 0.006 inch (perhaps smaller) may be used in controlled depth drilling, but drill breakage and cost increase with decreased diameter.

Laser drilling is gaining acceptance in the manufacture of high density interconnect (HDI) structures. In one manufacturing process, surface copper is patterned and etched at each hole location, and a CO_2 laser is used to ablate the dielectric, forming the hole over the pad below. Other processes combine the capability of an Excimer laser to remove copper and a CO_2 laser to ablate dielectric to form the holes. Laser drilling extends the limits of hole diameter beyond mechanical drilling, perhaps down to the 0.001- to 0.005-inch range at this time. As with mechanical drilling, the holes are formed sequentially, so that drilling time is directly proportional to hole count.

Plasma etching is an alternative to laser drilling, with all holes formed at the same time – an advantage with designs having a large number of holes. This process uses an RF-excited plasma, usually containing O_2 and CF_4, to attack non-reinforced dielectrics. A single-sided resin-coated foil, laminated to each side of a patterned core, is laminated with photoresist, imaged, developed, and etched to remove copper and expose the resin at desired hole locations. After stripping the photoresist, treatment by the plasma removes exposed dielectric, forming the holes to the pads on the layer below. Subsequently, hole metallization and patterning processes are performed to complete this subtractive approach to microvia fabrication.

Photodefined via technologies provide another alternative to laser-drilled microvias. Similar to the plasma process, all vias are formed simultaneously, but this is a semi-additive rather than a subtractive process. A permanent photosensitive dielectric is applied to a patterned core, and imaged and developed to form holes in the dielectric to the pads on the layer below. A swell-etch treatment is often required to roughen the permanent dielectric surface and provide adequate adhesion for subsequent metallization. Either panel plating or pattern plating may be used to complete the interconnection

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between the two layers.

Hole Quality

Many factors affect the quality of the finished holes. In mechanically drilled through-holes, entrance and backup materials are used to minimize entrance and exit burr. Drilling speed and feed rates are adjusted for optimum throughput, to extend drill life, minimize drill smear and nail heading on innerlayers, and provide smooth sidewalls. Worn drill bits will degrade the quality of the drilled holes. Depending on the diameter, the drill bits may be re-sharpened one or more times, extending their useful life while maintaining quality holes.

Unlike the mature technology of mechanical drilling, alternative technologies developed to accommodate the need for microvias have different issues. Often it is appropriate to ask the following questions: Has the hole been formed? Is the copper pad at the base of the hole clean? Is there a foot at the base of the hole that reduces the area of connection on the metal pad below? Is the shape of the hole acceptable for subsequent metallization?

Many manufacturers are exploring new technologies for forming microvias. During early stages of investigation, it is especially critical to address these issues, and discover the factors that contribute to failure and success. By exploring the processing parameters to determine the operating window and its impact on microvia quality, manufacturers can expedite the transition to a new technology.

Check for Residue at the Bottom of Microvias

A simple test prior to the metallization process can help to establish optimum processing parameters for microvia fabrication. Although the procedure is destructive, it can be used with test patterns to gage the performance of those technologies that drop microvias to pads below.

The test employs an oxidizing agent or stain to discolor exposed copper. The treatment should provide high contrast between treated and untreated copper. After the holes are formed, expose the panel to the staining process, and observe the color of the copper pad at the bottom of the microvias. If the copper is stained, the hole was formed properly. If a thin residue remained at the bottom of the microvia, the copper will remain unaffected by the staining process.

Summary

Until recently, mechanically drilled through-holes and vias have satisfied interconnection demands of most printed circuit designs. The technology is mature, well understood and reliable, but it is not a satisfactory solution for microvias.

The increased trends toward circuit miniaturization during the past few years have created a demand for alternatives to mechanically drilled microvias. As printed circuit manufacturers consider alternatives to conventional drilling, they must realize that these alternative technologies are relatively new, immature, and require development.

During the development and evaluation phase, fabricators need to determine optimum processing parameters that produce the highest quality microvias. Thin dielectric residue at the bottom of microvias is one defect that can be detected prior to metallization. A simple test, using an oxidizing agent or stain to discolor exposed copper can identify the presence of residues and help optimize process parameters expeditiously.

After establishing the optimum parameters for hole formation, test patterns may be metallized, patterned, and tested to evaluate additional steps in the process.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume V • Issue 3**

THE CHALLENGES FOR MICROVIAS

The seven previous columns were dedicated to *Investigating Process Capability*, with discussions on the preclean, photoresist application, imaging, developing, etching, drilling, and plating processes. In this column, data presented from five printed circuit manufacturers will emphasize the challenges ahead in the fabrication of microvias.

The Design

The process capability panel used in this study was a 10-layer 18" by 24" design, with one HDI layer on each side of an 8-layer core. The panel had conductor, via, and registration features designed within one-inch-square modules, and distributed over the panel surface. A two-mil-thick non-reinforced dielectric was specified for the HDI dielectric layers.

The microvia modules had four daisy-chain nets interconnecting layers 1 and 2. Each daisy chain within the design had 262 microvias, providing ample opportunity for failures to occur. The four daisy-chain designs within each module called for 6-mil maximum diameter microvias with 16, 14, 12, and 10-mil pads, respectively.

The HDI registration modules contained an array of 6-mil-diameter microvias that were designed with clearance to a conductive grid patterned on layer 2. The designed clearances ranged from 2.0 to 8.0 mils, in 1-mil increments. Electrical continuity measured between the microvias and the grid indicates that the misregistration of the hole relative to the layer below exceeded the designed clearance.

A total of 45 microvia modules and 8 HDI registration modules were distributed over the top surface of each panel. Each printed circuit manufacturer supplied 25 to 30 panels for the study.

Results

The analysis of the data is summarized by several key metrics: microvia defect density, mean resistance of the daisy-chain nets, resistance range of the daisy-chain nets, daisy-chain resistance coefficient of variation, and registration results. Results from 10-mil mechanically drilled through-hole daisy-chain nets and 20-mil mechanically drilled registration modules from the 8-layer core are included for comparison to conventional technology.

Microvia Defect Density

The microvia defect density, based upon "open nets," was calculated for panels submitted by each manufacturer. Considerable variation was measured among the five sets of panels. Figure 1 displays microvia defect density by manufacturer for each of the four daisy-chain designs fabricated by the manufacturers. There was no significant dependence of defect density observed as a function of land diameter. Since the requirement on microvia diameter was a maximum of 6-mils diameter, each manufacturer most likely kept the diameter constant.

Process A recorded the highest defect levels, greater than 550 defects per million vias (DMV) for each of the four pad sizes in the design. Processes B, C, and D performed much better than Process A, with defect levels ranging from 77 to 3 DMV. Process E performed best, fabricating more than 1,413,000 microvias with zero defects. For comparison, the dashed line in the figure is drawn at the defect density typical for 10-mil mechanically drilled vias.

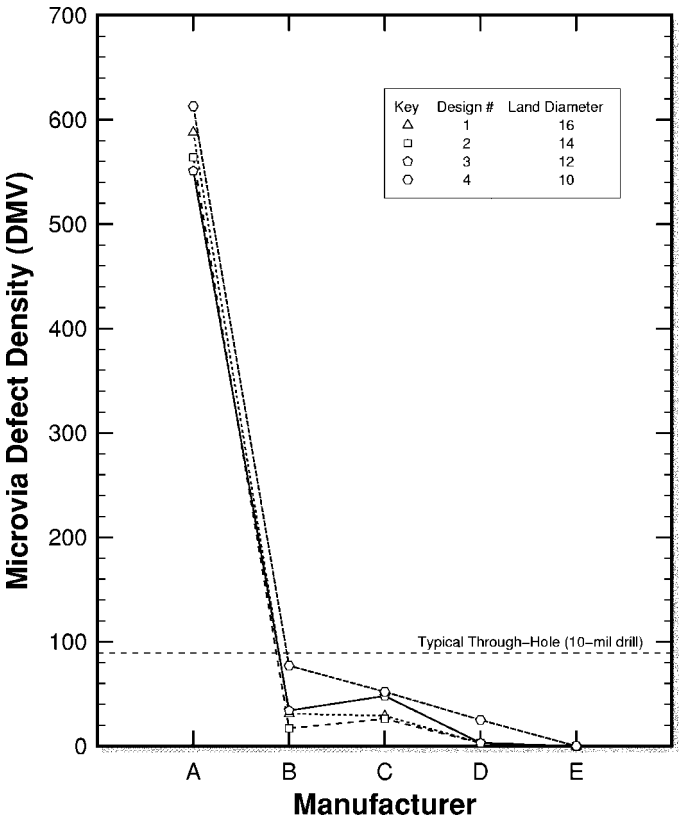

Figure 1. Microvia Defect Density by Manufacturer

Mean Resistance

The precision resistance measured from each daisy chain is used to evaluate the uniformity of the fabrication process. The mean resistance is an indicator of the plating thickness, land diameters, and track widths in the daisy-chain nets. Higher resistance values indicate thinner copper, smaller diameter lands, and/or narrower conductors, while lower resistance values suggest thicker copper, larger diameter lands, and/or wider conductors.

Figure 2 displays the mean resistance calculated for each daisy-chain design plotted by manufacturer. The mean values increased with smaller diameter lands, which was consistent among all manufacturers. Because the effective length of each 5-mil-wide track that connects adjacent lands increases as the land diameter decreases, this trend was expected.

The mean daisy-chain resistance varied significantly among

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the manufacturers. Manufacturer B recorded the highest values, ranging from 1195 to 1647 milliohms, while Manufacturer C had the lowest values, ranging from 475 to 584 milliohms. The major factor contributing to the differences is undoubtedly copper thickness, with Manufacturer B having much thinner copper than Manufacturer C. The typical average resistance for 10-mil mechanically drilled vias shown in the figure is 514 milliohms.

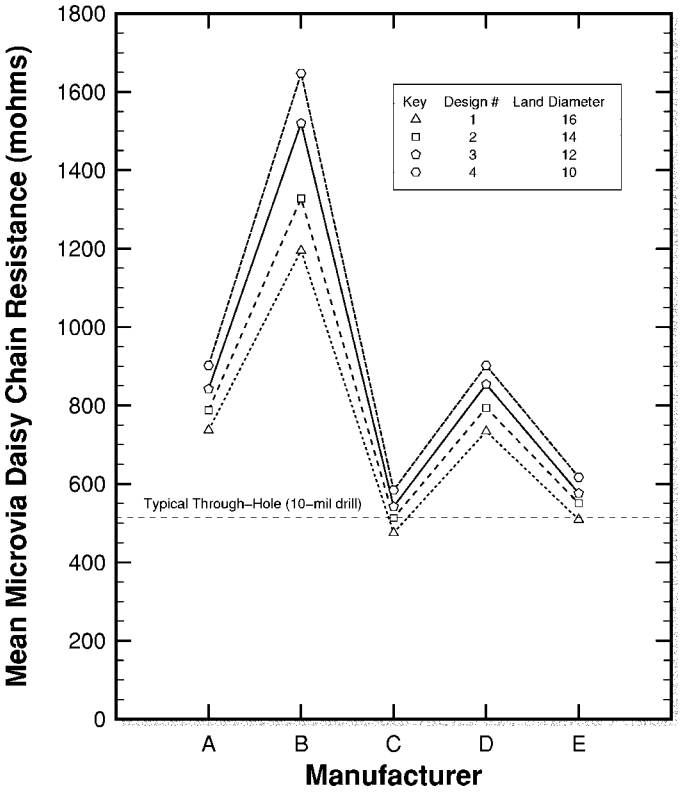

Figure 2. Mean Microvia Daisy Chain Resistance

Resistance Range

The range in microvia daisy-chain resistance, defined as the maximum minus the minimum resistance within each of the four land diameters, is shown in Figure 3. This data tracks the mean data, with larger means having larger ranges. However, Manufacturers C, D, and E had resistance ranges that were approximately one-half the mean value, while Manufacturers A and B had ranges that were one to two times the mean. The typical 10-mil diameter mechanically drilled via recorded a range of 193 milliohms, less than any of the microvia designs.

Resistance Coefficient of Variation

The coefficient of variation (CoV), defined as the standard deviation divided by the mean expressed in percent, is a measure of the variation relative to the mean. Figure 4 shows the CoV for each land diameter plotted by manufacturer. Clearly, the uniformity of via daisy chains fabricated by Manufacturer A, and especially B were much worse than that of Manufacturers C, D, and E. The uniformity of the typical 10-mil diameter through-hole recorded a CoV of just over 4 percent, much less than the best microvia designs.

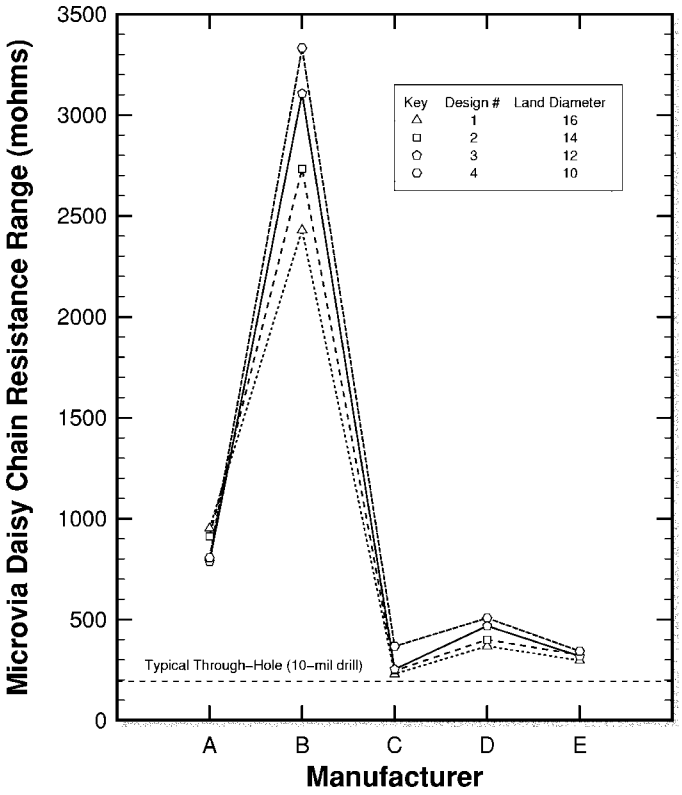

Figure 3. Microvia Daisy Chain Resistance Range

Registration Results

Registration is a controlling factor that affects circuit density. Designed clearances between features must take into account process variation – effectively decreasing density, or risk potential yield and reliability failures. The placement of holes relative to features patterned on conductive layers depends upon material movement and distortion, tooling methodology and capability, hole positioning accuracy, etc. Circuit density is controlled by the land diameter required to capture the microvia (taking registration capability into account), in conjunction with minimum clearance requirements.

The registration results from the five printed circuit manufacturers are shown in Figure 5. The raw data acquired from the process capability panels are converted to parameters important to production. Percent of holes without breakout is plotted versus annular ring for each manufacturer. The typical plated-through-hole capability based on drilled hole to signal layer registration capability from the 8-layer core is shown in the figure for comparison.

The typical plated-through-hole capability was worse than any of the HDI processes. The misregistration and distortion that occurs during the lamination of the core, cause the four

internal signal layers to shift relative to each other, and consequently contribute to lower capability. The HDI processes did not have this factor contributing to misregistration. Manufacturer A performed best among the participants, recording nearly perfect registration for all designed clearances. Manufacturer C was second to A, with the data predicting 87 percent of 2-mil annular rings without breakout. Manufacturers D and E followed behind C, and Manufacturer B performed the worst, with the data predicting 18-, 55-, 81-, 95, and 98 percent of 2-, 3-, 4-, 5-, and 6-mil annular rings without breakout respectively.

To emphasize the importance of this data in terms of circuit density, both Manufacturer D and E will require annular rings of at least 5 mils in order to ensure no breakout. This translates to a 16-mil pad with a 6 mil via.

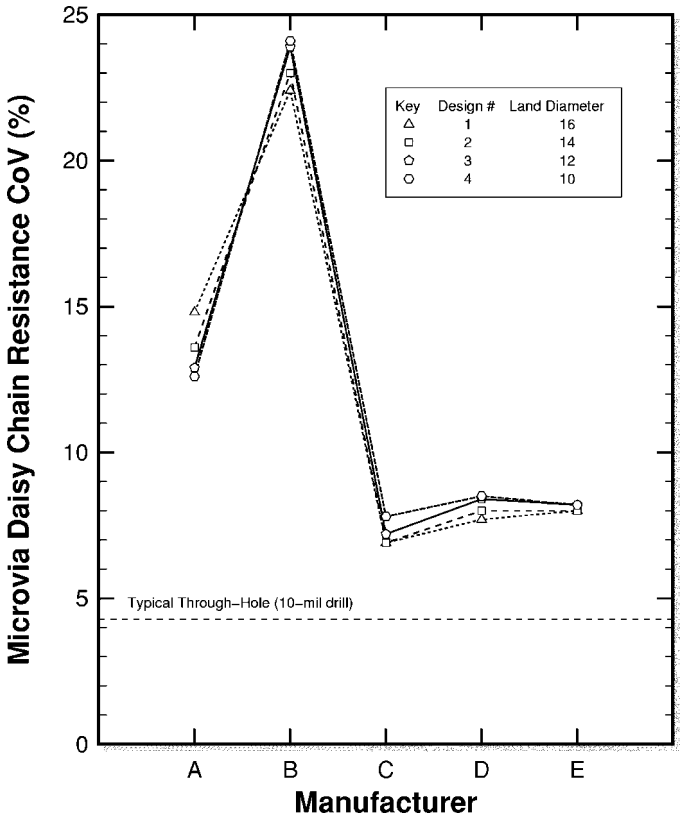

Figure 4. Microvia Daisy Chain Resistance CoV

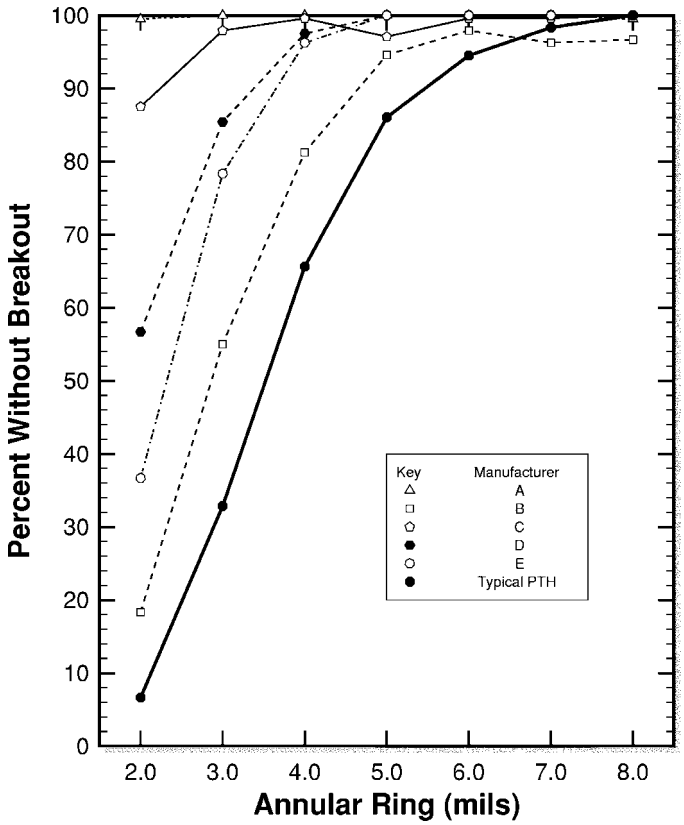

Figure 5. HDI Registration Results

Summary

Results from five manufacturers indicate a wide range in capability and quality, quantified in terms of defect density, uniformity, and registration capability. The formation of microvias and the cleaning processes they receive in preparation for metallization are demanding. The holes must be properly formed, and extend to the pad on the buried layer. They must be free of debris and other contaminants, and the copper surface on the pad below must be clean as well. Perhaps more challenging is the metallization process itself, which must deposit copper on the hole sidewalls and provide dependable electrical connection to the pad on the layer below.

Defect levels and uniformity results from the five manufacturers in this study indicate that the holes are not formed and cleaned consistently, nor are they metallized uniformly. Manufacturers are faced with new challenges when asked to fabricate microvias. To realize the benefits, land diameters must be small, registration must be improved, and microvia formation, cleaning, and metallization must become more robust.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume V • Issue 4**

AN ASSESSMENT OF MICROVIA RELIABILITY

Some of the challenges facing manufacturers when fabricating microvias were discussed in the last column. The hole formation, cleaning, and metallization processes must be robust to achieve successful interconnection. In this column, the discussion centers on the reliability of microvias when exposed to an assembly simulation process. The thermal excursions from the assembly simulation process caused some vias to fail, while large changes in resistance were measured in others.

Process Capability Panel Design

The process capability panel used in this study was a 24-layer design on an 18" by 24" format. The 16" by 22" active area of the panel was covered with 352 one-inch-square modules with conductor and space, via, or registration features. The microvias were laser-drilled through 3.5 mils of dielectric from Layer 1 to 2 and 24 to 23, and through 7 mils of dielectric from Layer 1 to 3 and 24 to 22.

Figure 1 is a schematic showing the locations of the microvia modules on the panel surface. The lighter-shaded modules have microvias from Layers 1-2 and 24-23, while the darker-shaded modules have microvias from Layers 1-3 and 24-22. The unshaded modules contain conductor and space, registration, and through-hole via features.

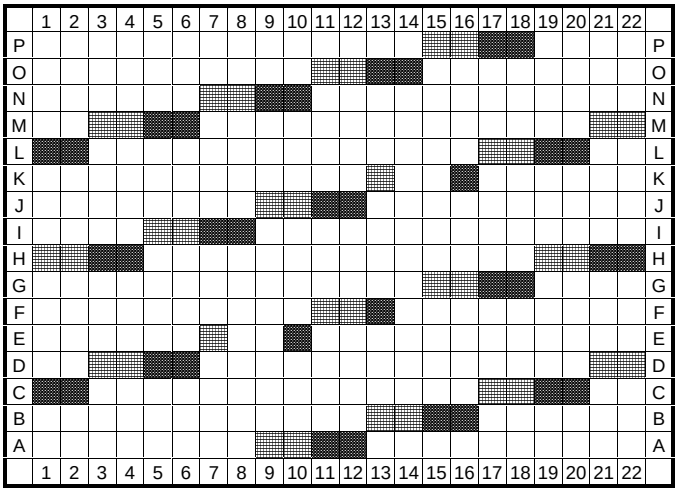

Figure 1. Process Capability Panel Schematic

Each microvia module contains four daisy-chain nets, forming a conductive path between the two associated layers. Figure 2 shows a schematic of one via module, extending from Layer 1 to 2. Table 1 summarizes the feature sizes and via counts of the two module designs. There are 72 modules per panel having microvias formed in 3.5-mil-thick dielectric, and 70 modules per panel having microvias formed in 7-mil-thick dielectric.

Procedure

Twenty panels, fabricated by one manufacturer, were tested and analyzed for conductor and space defect density and conductor width and height uniformity, via yield and uniformity, and registration capability. Two of these panels were selected for additional tests to ascertain microvia reliability. The panels were subjected to two passes through an infrared (IR) oven to simulate thermal excursions experienced during assembly. Following the assembly simulation, the panels were re-tested to determine the changes that occurred from exposure to the IR stress.

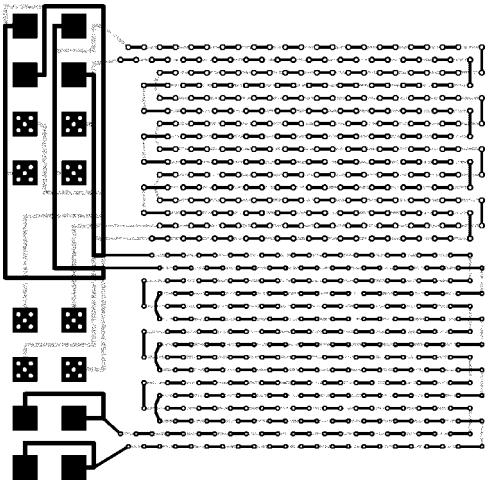

Figure 2. Schematic of the Via Daisy-Chain Module

Vias Connecting Layers	Hole Diameter (mils)	Land Diameter (mils)	Number Vias per Net	Number Vias per Panel
1-2 & 24-23	6	12	170	12,240
	5	12	170	12,240
	4	10	170	12,240
	3	10	170	12,240
1-3 & 24-22	8	14	170	11,900
	7	14	170	11,900
	6	12	170	11,900
	5	12	170	11,900

Table 1. Microvia Design Information

Results

Changes in yield and resistance occurred as a result of the assembly simulation process. Figure 3 shows via net yield plotted versus nominal hole diameter for vias formed in 3.5- and 7-mil-thick dielectric, before and after stress. The microvias formed in 3.5-mil dielectric, extending from Layers 1-2 and 24-23, initially had high yields, with one additional "open" in the 3-mil diameter microvia daisy chain occurring after IR stress. The 5- and 6-mil-diameter microvia daisy chains formed in the thinner dielectric recorded 100 percent yield.

Doubling the dielectric thickness lowered the yields for 5- and

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6-mil-diameter microvia daisy chains, with performance reduced to approximately 14 percent. The 8-mil-diameter via daisy chains had just one "open" net prior to stress, and one additional "open" after stress. The 7-mil-diameter via daisy chains exhibited poorer performance, with 11 additional "opens" due to the IR stress, dropping the yield to 60 percent. For via height-to-diameter aspect ratios of 0.7 and lower, performance was very good. As the aspect ratio increased, performance degraded, with the sharpest decline occurring in vias formed in the thicker dielectric.

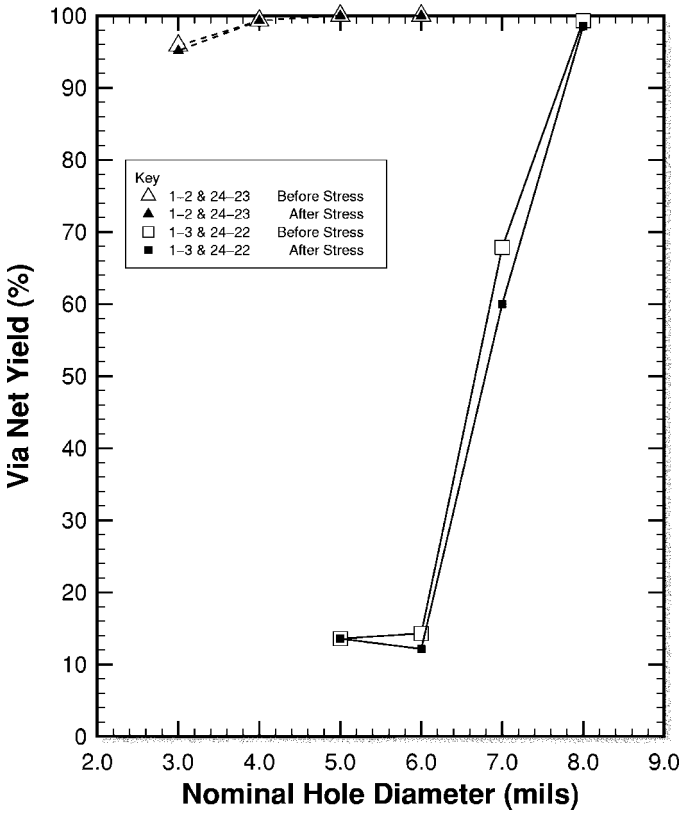

Figure 3. Via Net Yield Before and After Assembly Simulation

The change recorded in the daisy-chain resistance provides additional insight into the quality of the microvias. While a number of additional "opens" resulted from the IR assembly simulation process, changes in daisy-chain resistance indicate marginal interconnections in some of the remaining functional chains. Figure 4 shows the relative change in via net resistance plotted versus hole diameter for microvias formed in 3.5-mil thick dielectric, while a comparable graph for vias formed in 7-mil thick dielectric is shown in Figure 5. The distribution of the data is illustrated by notched box plots for each nominal hole size. The 6- and 5-mil-diameter microvias formed in the thin dielectric showed very small changes resulting from the IR stress. While data from the 4-mil diameter microvias exhibited slightly greater change than the larger holes, the 3-mil microvias clearly show a much broader distribution, suggesting reliability problems.

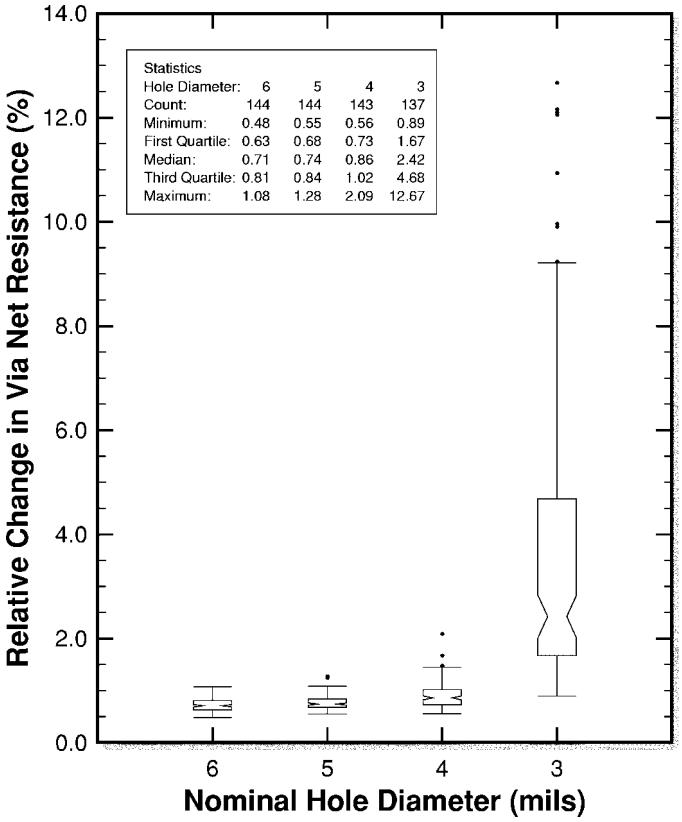

Figure 4. Relative Change in Via Net Resistance Layers 1-2 and 24-23

The results from the 7-mil-thick dielectric, shown in Figure 5, are dramatically worse. The arrows at the top of the graph indicate the number of data points that exceed the maximum scale. The maximum relative changes were 378, 1424, 570, and 363 percent for the 8-, 7-, 6-, and 5-mil diameter vias, respectively. Clearly, development work is needed before laser-drilled vias of this size are viable in 7-mil-thick dielectric.

Summary

Laser drilling is one method used to form microvias in printed circuit boards. Results from tests of process capability panels with 5- and 6-mil-diameter laser-drilled microvias formed in 3.5-mil-thick dielectric show good capability. These larger diameter microvias performed well when subjected to an assembly simulation process, without failures and very small changes in the resistance of the daisy chains. The 3-mil-diameter microvias experienced one additional failure, and significantly greater relative change in daisy-chain resistance resulting from the thermal stress.

Results for 5- and 6-mil-diameter microvias formed in 7-mil-thick dielectric were very poor. Changes in daisy-chain

resistance due to the thermal stress were significant for all via sizes formed in the thicker dielectric. Before capability is established for laser-drilled vias in 7-mil dielectric, additional development work is required.

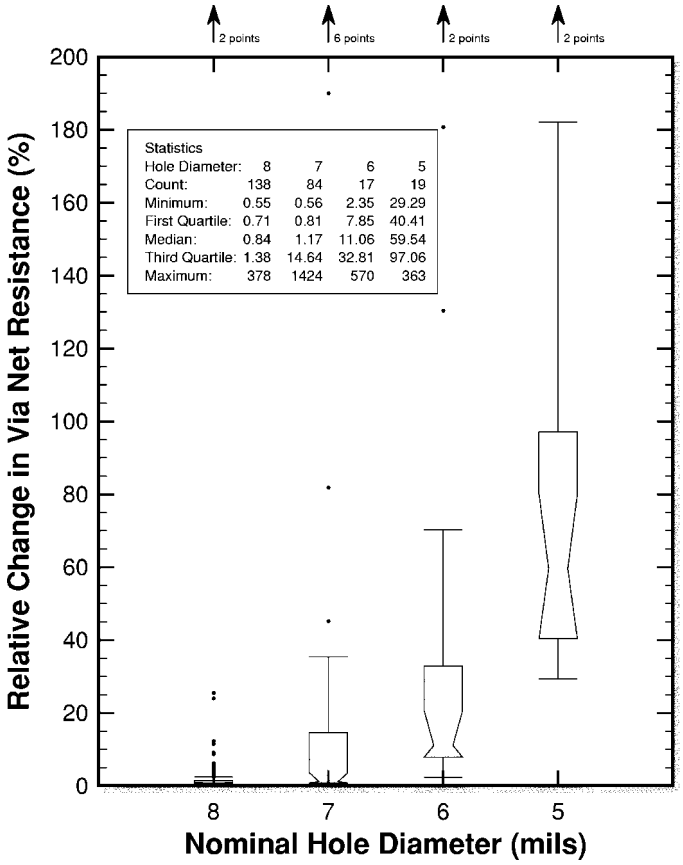

Figure 5. Relative Change in Via Net Resistance Layers 1-3 and 24-22

The process capability panels, electrical test, and data analysis techniques used in this study may be applied to any microvia development or screening effort. When used with environmental stress, such as the simulated assembly process, the technique offers a useful method to optimize processing and design parameters. After an acceptable fabrication process has been established, in-depth accelerated aging reliability studies using these techniques can be used to determine long-term reliability.

Acknowledgement

CAT Inc. would like to thank David Evans of Teradyne Inc., Agoura Hills, CA, and Wayne King of Teradyne Inc., San Jose, CA, for their contributions to this column.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume V • Issue 5**

ETCHER PERFORMANCE IMPROVEMENTS

In the absence of significant technological advancements in the manufacture of printed circuits, incremental improvements in every process step will be necessary to satisfy the demands of miniaturization as we enter the next millennium. The etching step, which forms the conductive paths on the substrate surfaces, is one process that can impart significant variation on conductor widths and adversely influence the performance of the finished product. It is difficult – if not impossible, to improve a process without relevant and meaningful data. Discussion in this column focuses on techniques to characterize treatment uniformity that are combined with designed experiments to benchmark and improve an innerlayer etcher.

Test Pattern

The process capability panel used in this study was a double-sided 18" by 24" panel with 352 one-inch-square modules on each side, arranged in 16 rows and 22 columns. Each module contained a multi-pitch, serpentine-shaped conductor pattern with 4-, 5-, 6-, and 7-mil-wide conductors, separated by 4-, 5-, and 6-mil-wide spaces, respectively. Each conductor within the module was approximately 17" in length.

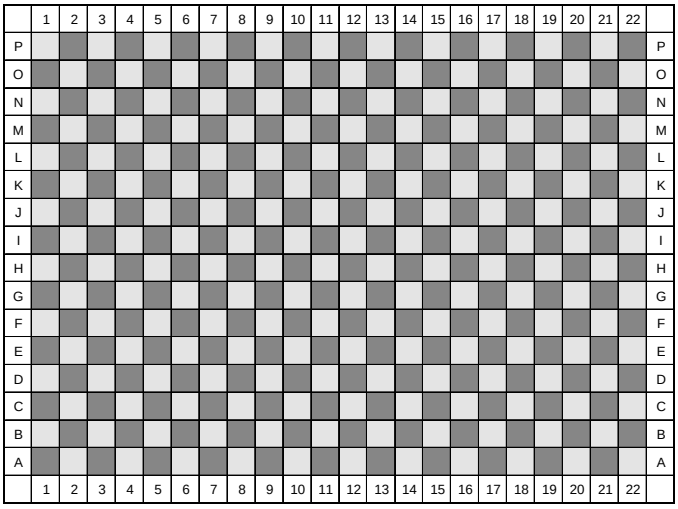

Figure 1. Schematic of the Process Capability Panel

Figure 1 displays a schematic representation of the process capability panel. The modules are arranged in a checkerboard pattern, with conductors running predominantly in a horizontal (parallel to the 24" edge) or vertical (parallel to the 18" edge) direction. Figure 2 shows a schematic rendering of the conductor module, oriented in the horizontal direction.

Testing Protocol

The investigation into etcher performance was accomplished by performing a variety of designed experiments. Each test required manufacturing a set of process capability panels, electrically testing the panels to acquire precision resistance from each conductor in the pattern, and an analysis of the data to establish treatment uniformity.

Some of the variables that were studied include transport speed, oscillation rate, spray pressure, acid normality, conveyor wheel spacing and count, and spray nozzle configuration.

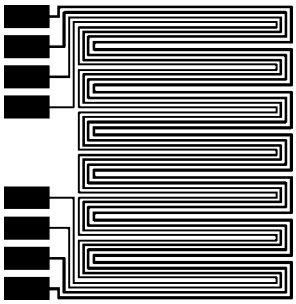

Figure 2. Schematic of a Conductor Module

Initial Performance

Initially, a set of six process capability panels was processed to establish performance prior to making any changes. The results showed significant variation over both the top and bottom surfaces of the panels. Figure 3 shows average conductor width loss over the top side of the panels. Conductor width loss is defined as the difference between the artwork feature width and the width calculated from the electrical resistance. The three-dimensional plot shows the conductor width loss at each module location, averaged over the top side of the six panels in this set. The target conductor width loss was 1.0 mils for all panels.

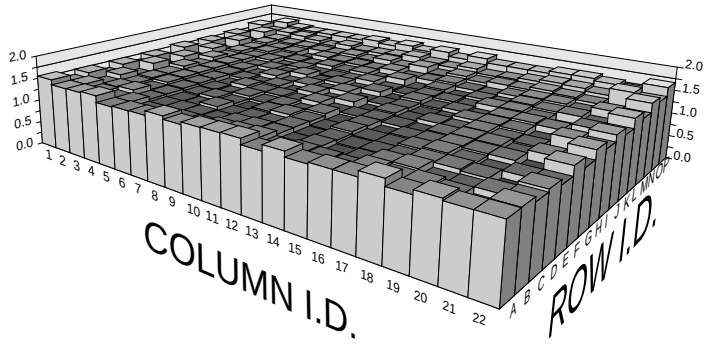

Figure 3. Conductor Width Loss - Top Sides, Before Changes

The three-dimensional plot shows the effect of puddling on the top side, a characteristic of all horizontally-transported etching systems. Greater etching occurred at the perimeter of the panels compared to the middle, causing the conductors at the perimeter to be narrower than those located at the center of the panel.

Conductor width loss was also dependent on the orientation of the conductors, particularly those located at the perimeter of the panel. In general, conductors oriented horizontally experienced greater line width loss than those oriented vertically.

The minimum, mean, and maximum conductor width loss for

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the top side of the panels measured 1.11, 1.34, and 1.68 mils, respectively, with a standard deviation of 0.11 mils.

The bottom side of the initial six panels exhibited striping in the transport direction, with a strong dependence on conductor orientation. These results are displayed in the three-dimensional plot shown in Figure 4. Notice that the checkerboard effect in Figure 4 corresponds to that of Figure 1. Once again, modules with conductors running horizontally experienced greater conductor width loss than those running vertically.

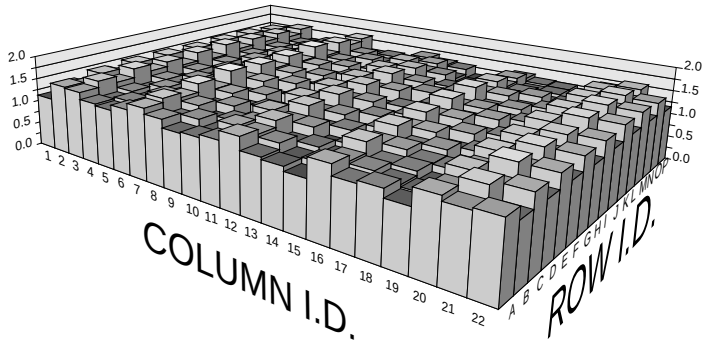

Figure 4. Conductor Width Loss - Bottom Sides, Before Changes

The minimum, mean, and maximum conductor width loss for the bottom side of the panels were 1.02, 1.37, and 1.76 mils, respectively, with a standard deviation of 0.16 mils.

Performance after Changes

The designed experiments resulted in changes to conveyor transport speed, oscillation rate, spray pressure settings, conveyor wheel spacing and count, and a redesign of the spray bars. Improvements were significant on the both sides of the panels.

Figure 5 shows the average conductor width loss from the top side of seven panels. While evidence of puddling is seen, the impact is reduced in comparison to the initial test. A small horizontal-to-vertical etching bias is also observed in this set of panels.

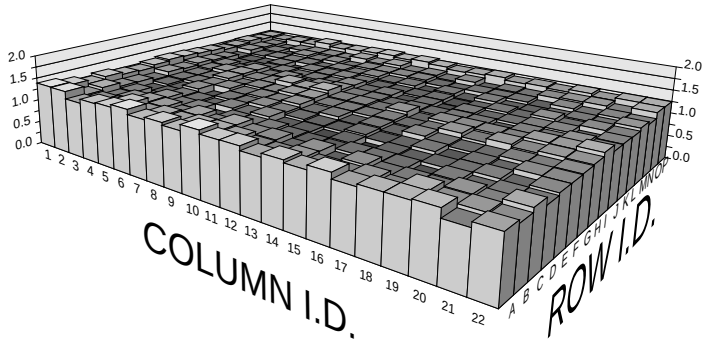

Figure 5. Conductor Width Loss - Top Side, After Changes

The minimum, mean, and maximum conductor width loss from the top side of this set were 0.93, 1.14, and 1.39 mils, respectively, with a standard deviation of 0.079 mils. The effects from both puddling and conductor orientation have been reduced, leading to improved uniformity and a mean conductor width loss closer to the 1.0-mil target.

Figure 6 illustrates significant improvement in treatment uniformity on the bottom side of the panels from this set. The striping that was observed in the initial run is nearly eliminated. Column 22 experienced the smallest conductor width loss, perhaps resulting from a clogged nozzle or unbalanced spray nozzles. A minor adjustment will improve this problem.

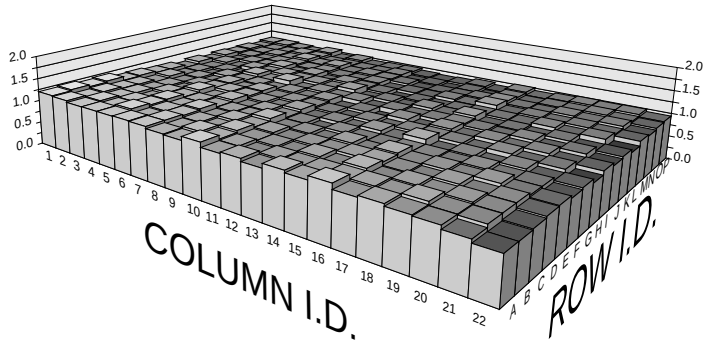

Figure 6. Conductor Width Loss - Bottom Side, After Changes

A weak horizontal-to-vertical conductor width loss bias is still observed on the bottom side of the panels, but the variation is much smaller than that of the initial run.

The minimum, mean, and maximum conductor width loss from the bottom side of the panels in this set were 0.83, 1.02, and 1.23 mils, respectively, with a standard deviation of 0.071 mils.

Summary

In the absence of technological advancements, circuit miniaturization requires incremental improvements in all manufacturing process steps. Relevant and meaningful data are necessary to characterize and improve a process. Designed experiments based around the manufacture, test, and analysis of process capability panels provide the data to study the etching process, optimize processing parameters, and redesign portions of the equipment. The equipment manufacturer will reportedly incorporate these design changes into future designs.

While additional studies may lead to further improvements in treatment uniformity, significant progress was achieved. The major factors contributing to variation were puddling on the top side, and striping and horizontal-to-vertical orientation etching bias on the bottom side. By implementing the changes, the top side standard deviation decreased from 0.11 mils to 0.079 mils, and the bottom side standard deviation decreased from 0.16 mils to 0.071 mils.

Acknowledgements

The author graciously acknowledges the contributions of Gerald Cessac and Tim Estes for running the designed experiments that led to the improvements reported here.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume V • Issue 6**

THE IMPACT OF SUBTLE PROCESS VARIATIONS

The last column focused on measuring and improving treatment uniformity of an innerlayer etcher. Designed experiments run in combination with specialized measurement and analysis techniques, lead to process and design changes that result in improved conductor width uniformity.

In addition to conductor width, the height of the finished conductor is important, especially as features become smaller. Similar to conductor width, the conductor height affects the current-carrying capability, the impedance, and the reliability of the completed circuit. This column examines variations in innerlayer conductor height, and suggests possible sources of the variations. PCB fabricators and their customers may be unaware that the problem exists, which may cause some product to fall short of specification.

Possible Sources of Conductor Height Variation

Copper clad laminate is available from suppliers in a range of weights. One-ounce (one-ounce per square foot is nominally 1.4 mils thick) and half-ounce copper are commonly used in innerlayer applications, but thinner and thicker versions are readily available as well. The copper foils are typically fabricated by an electroplating process, treated with an adhesion promoter, and laminated to C-stage dielectric. Often, an anti-tarnish treatment is applied to the copper by the vendor. Small variations in copper thickness are to be expected from the vendor.

The PCB fabricator will remove the anti-tarnish treatment if present, and process the innerlayer cores through a cleaning process to promote adhesion prior to photoresist application. Depending upon the cleaning process employed, copper thickness may be reduced from 0.0 to 0.1 mils – sometimes even more.

On occasion, some fabricators will strip the imaged and developed photoresist from defective innerlayer cores, and reprocess the cores, beginning with the preclean process. This practice can lead to additional loss of copper, resulting in reduced conductor height.

Data from a 12-layer Process Capability Panel

Variation in innerlayer copper thickness was measured in a set of ten 12-layer 18" by 24" process capability panels. The data are from serpentine-shaped conductor patterns arranged in one-inch-square modules, and dispersed over the surfaces of the innerlayers. Precision electrical resistance measurements were obtained from 37 to 39 modules on each innerlayer, and the copper thickness was calculated for each module using proprietary analysis techniques.

Figure 1 is a graph of conductor height versus panel number for half-ounce innerlayers 4, 5, 8, and 9. The data are displayed as notched box plots, with the median centered on the notch, the box extending from the first to the third quartile, and the bars extending to the lower and upper adjacent values. Clearly, the results from panels 1-3 are significantly different from panels 4-10.

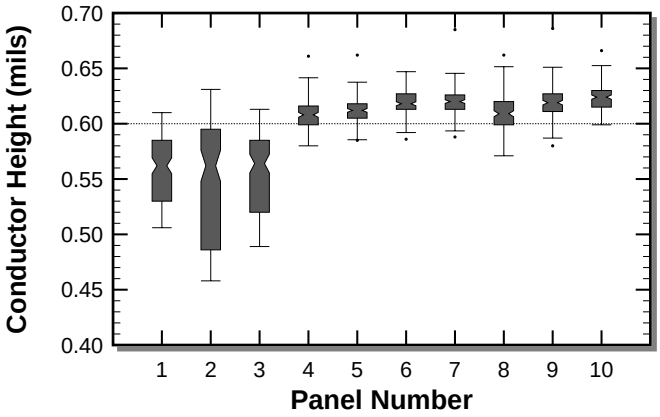

Figure 1. Conductor Height by Panel - Innerlayers 4, 5, 8 & 9

The source of the large variation in panels 1-3 is revealed by examining the results from innerlayers 4 and 5 (fabricated on one core) separately from innerlayers 8 and 9 (fabricated on another core.)

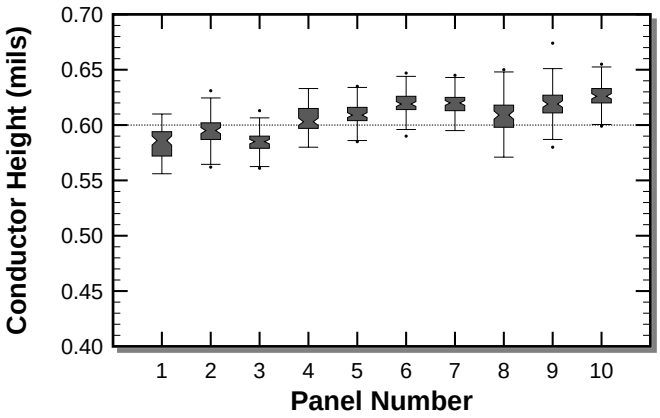

Figure 2. Conductor Height by Panel - Innerlayers 4 & 5

Figures 2 and 3 show the conductor height plotted versus panel number for innerlayers 4 and 5, and innerlayers 8 and 9, respectively. Although innerlayers 4 and 5 exhibit a trend of increased conductor height with panel number, the distribution is similar for each panel. If the cores were precleaned in panel-number sequence, the trend may indicate a decrease in activity of the cleaning process with increased loading. Alternatively, the trend could be a coincidence, and the variations reflect the variation in copper thickness supplied by the vendor.

Results from innerlayers 8 and 9 show significantly thinner conductor height in panels 1-3 compared to panels 4-10. It is highly unlikely that the source of this variation is the laminate supplier. The variation is probably due to reprocessing cores

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that were found defective after photoresist exposure and development. The stripping and extra cleaning processes removed additional copper, accounting for the variation.

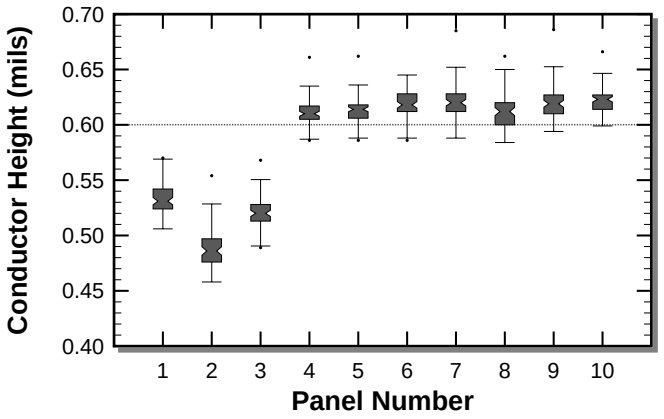

Figure 3. Conductor Height by Panel - Innerlayers 8 & 9

The Impact

Innerlayers 8 and 9 in panels 4-10 recorded an average conductor height of 0.62 ± 0.014 mils, 0.08 mils less than the nominal thickness of half-ounce copper. Results for panels 1-3 showed an average conductor height of 0.51 ± 0.025 mils for innerlayers 8 and 9, a reduction of 0.19 mils from the nominal thickness. However, the minimum conductor height in panels 4-10 was 0.58 mils compared to 0.46 mils for panels 1-3. A reduction of 34 percent in conductor height from nominal for panels 1-3 might exceed allowable specification limits, adversely affect impedance, and introduce threats to product reliability.

Summary

Conductor height impacts current-carrying capability, impedance, and reliability of the finished circuits. Sources of variation begin with the laminate supplier, where small variations in copper thickness are to be expected. Some cleaning processes, implemented by PCB fabricators to remove anti-tarnish treatments and promote adhesion between the photoresist and copper, can remove 0.1 mils of copper or more. More important than average thickness, the minimum copper thickness represents the worst case condition, and is influenced by preclean treatment uniformity.

Half-ounce copper clad cores fabricated as innerlayers in seven 12-layer process capability panels recorded an average conductor height of 0.62 ± 0.014 mils, with a minimum height of 0.58 mils. Innerlayer cores fabricated in three process capability panels from the same lot recorded conductor heights of 0.51 ± 0.025 mils, with a minimum height of 0.46 mils. The cores with thinner copper were most likely identified as defective after imaging and developing, and were reprocessed rather than scrapped.

Fabricators who reprocess cores that are found to be defective after photoresist imaging and developing, should characterize their preclean process to ascertain the impact on finished conductor height. Depending upon the aggressiveness of the preclean process, fabricators should consider scrapping rather than reprocessing innerlayer cores – especially those with thinner vendor copper.

OEMs who purchase PCBs should be aware of this issue, and insist on scrapping in favor of reprocessing innerlayer cores in critical applications.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume V • Issue 9**

SOLDERMASK REGISTRATION

Original equipment manufacturers (OEMs) and contract electronics manufacturers (CEMs) purchase printed circuit boards from merchant suppliers. Since capability, quality, delivery, and price vary significantly among suppliers, OEMs and CEMs are gathering quantitative data indicative of capability and quality as part of the supplier management process. Previous columns have included data confirming diverse capabilities among suppliers to fabricate narrow conductors and spaces, form and metallize microvias, maintain tight registration, and fabricate controlled impedance circuits.

This month, soldermask registration is discussed. Similar to most parts of the printed circuit fabrication process, advancements in packaging technologies are pushing toward tighter soldermask registration requirements. Results from supplier management studies show a wide range in soldermask registration capability among 13 participating fabricators.

Soldermask Registration Requirements

Many soldermask materials are available to the industry. Liquid soldermasks may be applied by screen printing, curtain coating, roller coating, and spray coating processes. Dry film soldermasks are applied by hot roll vacuum laminators.

Patterning the soldermask can be accomplished by screen printing, but applications requiring higher resolution (smaller features and tighter registration) usually rely on photoimageable liquid or dry film materials. In the highest density applications, the soldermask may be ablated by laser to form the pattern.

While soldermask provides many physical, environmental, and electrical benefits, the main function of soldermask is to prevent bridging (shorts) between conductors. Soldermask covers and protects conductive surfaces, leaving openings to pads for subsequent interconnection to packages. To be effective, the openings in the soldermask must be closely registered to surface mount pads corresponding to the footprints of the packages mounted on the circuit board. As packaging density increases, surface mount pads become smaller, with decreased spacing from pad-to-pad. While registration requirements depend upon the design of the circuit board, typical required placement accuracy is on the order of ± 3 mils, with tighter applications requiring ± 2 mils and the highest density applications approaching ± 1 mil.

Soldermask Registration Module

A schematic of the soldermask registration module is shown in Figure 1. The large pads at the left of the module are probed by the test system to measure continuity. Conductor traces patterned on the outerlayer, running from the four lower pads, connect to seven copper bars. Each bar has 16 circular antipads that provide a nominal clearance between a 20-mil diameter opening in the soldermask and the copper bar. After fabrication is complete, conducting silver ink is applied in the soldermask openings and along the surface of the soldermask above each copper bar. The conductive path is extended from each clearance bar to the appropriate pad, which is connected to one of the four large pads at the upper left of the module. The designed clearances investigated in this study were 2.0 to 4.5 mils in 0.5-mil increments.

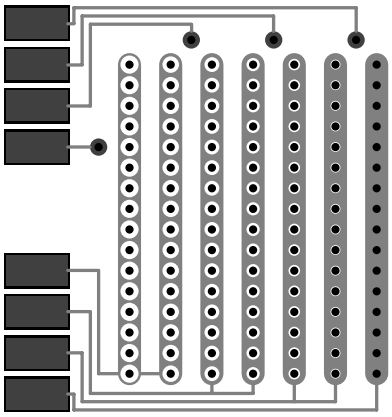

Figure 1. Soldermask Registration Module

The antipads in the right-most bar of the module were smaller than the openings in the soldermask to provide a 1.0 mil interference that is designed to be "shorted" and confirm that design dimensions were met. All other tests for continuity should be "open circuit" for a clearance that is maintained, and "short circuit" for a misregistration equal to or greater than the designed clearance.

As a part of the supplier management procedure, an OEM investigated the soldermask registration capability of 13 suppliers. Eight one-inch-square soldermask registration modules were incorporated on the process capability panel: four on the top side and four on the bottom side. Each supplier manufactured a total of 30 panels, providing a population of 240 registration tests for each designed clearance.

Results

Figure 2 is a graph of clearance yield versus clearance for the printed circuit board fabricators. Clearance yield is defined at each nominal clearance as 100 multiplied by the number of tests that maintained isolation divided by the total number of tests. The results reinforce the concern of OEMs regarding adequate soldermask registration capability among suppliers. Some of the fabricators performed well across the range of clearances from 2.0 to 4.5 mils, while others recorded poor registration capability, especially at the narrower clearance values. Of all the suppliers, however, only supplier 'F' recorded 100 percent clearance yield at the largest nominal clearance of 4.5 mils. All suppliers participating in this study fell short of achieving the typical registration requirements of ± 3 mils.

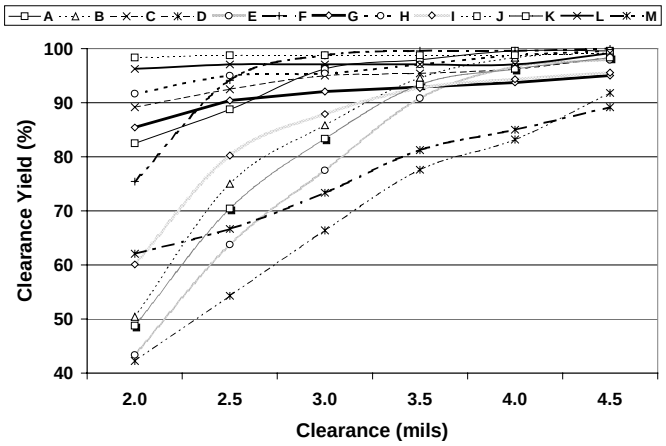

Figure 2. Soldermask Registration Results

Summary

As a part of the supplier management process, OEMs and CEMs are gathering quantitative data from PCB suppliers to ensure the highest possible quality in their products. Soldermask registration requirements are driven by the density of packages used in electronic assemblies, and are becoming more stringent. Typically, soldermask features require registration to within ± 3 mils, with more advanced packaging requirements of ± 2 mils and even down to ± 1 mil.

Results from 13 suppliers participating in an OEM supplier management activity show a wide range in soldermask registration capability. While there were clearly differences in capability among the suppliers, none displayed the capability to achieve the typical requirement of ± 3 mils. As requirements become more stringent, suppliers may have to replace photoimageable soldermask with materials that may be patterned by laser ablation.

Acknowledgements

CAT Inc. would like to thank Rick Snyder of Delphi Delco Electronic Systems and Happy Holden of TechLead Corporation for discussions on soldermask requirements. Further, we gratefully acknowledge Happy Holden for the soldermask registration test vehicle design concept that he and others developed while with Hewlett Packard.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume V • Issue 10**

VIA CAPABILITY AND QUALITY

The registration, formation, cleaning, metallization, and patterning processes used in the fabrication of vias must be accomplished with precision to achieve the level of quality required in today's printed circuits. Blind vias present particularly challenging problems, especially as hole sizes decrease and hole aspect ratios increase. With improved registration, smaller vias, and smaller lands, the number of vias per board will undoubtedly increase. The dilemma resulting from miniaturization is that these more difficult-to-fabricate vias must be manufactured at lower defect levels to achieve equivalent yields.

This column will introduce the concepts of capability and quality in the manufacture of vias in printed circuit boards. The next column will discuss results of a supplier management program that included nine manufacturers. Data from through vias, and blind vias formed in two- and four-mil-thick dielectric (more than 7 million vias total) will emphasize the difficulty of fabricating blind vias, and show a wide range of capability and quality present in the industry.

New materials, equipment, and processes are being developed and implemented to fabricate microvias at high yield in production. Long-term reliability of products manufactured with unproven processes must be established. The last column of this three-part series will show that capability and quality must be achieved before initiation of long-term reliability studies.

Via Modules

Via modules are designed to provide spatially-dependent quantitative data on yield, defect density, and uniformity from localized areas of Process Capability Panels. The modules are one-inch square with four daisy chain nets covering the module area. The interconnection sequence that the daisy chain traverses is based upon the multilayer structure investigated, and the chain may bounce between two or more layers. Each net is designed with a unique hole/land combination to investigate the impact of feature sizes on performance. Figure 1 shows a schematic of a via module forming a daisy chain between two layers. Precision electrical resistance measurements from each daisy chain provide the data to calculate defect density and quality of the vias.

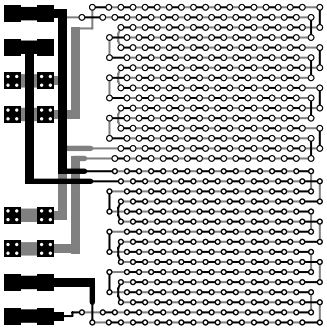

Figure 1. Schematic of a Via Module

Via Defect Density

A Poisson model is used to calculate via defect densities and predict yield on product. The via defect density, reported in defects per million vias, is calculated by Equation 1,

$$\lambda = -10^6 \{\ln Y'\}/n \quad (1)$$

where Y´ is the number of good daisy chains divided by the total number of daisy chains, and n is the number of vias in each daisy chain.

Upon establishing the defect density of a specific manufacturing process, predicted yield on product is calculated by Equation 2,

$$Y = 100\, e^{-\lambda N} \quad (2)$$

where N is the total number of vias in a board. Figure 2 shows the impact of defect density on product yield. Predicted product yield is plotted versus number of vias. The five curves in the figure are based on defect densities of 50, 100, 200, 500, and 1000 defects per million vias.

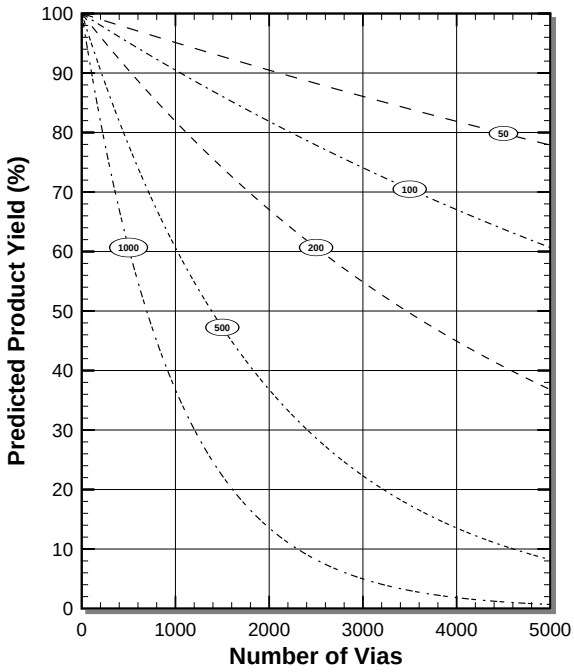

Figure 2. The Impact of Defect Density on Product Yield

For designs having modest numbers of vias, a higher defect density can be tolerated than in designs with high via counts. A board with 200 vias manufactured by a process with a defect density of 500 defects per million vias, for example, will have the same yield as another board with 2000 vias manufactured by a process running at 50 defects per million vias – both will have 90 percent yield. However, for boards with 2000 vias, the yield drops significantly (from 90 percent to 37 percent) as the defect density increases from 50 to 500 defects per million vias. High defect densities translate directly to increased scrap, leading to additional costs and shipping delays.

Via Quality

Once the vias have been fabricated successfully, the quality of the vias in the chain can be characterized by precision resistance measurements. Each daisy chain net within a module is replicated over the surface of the panel, from one side to the other (in the case of blind vias), and from panel to panel. Since the physical designs are identical, the precision resistance for each unique net should have the same value. Variations in resistance stem from registration errors, hole formation and cleaning differences, plating and etching differences, and the quality of the interfaces formed during plating processes between innerlayers and hole wall barrels, and between pads and copper plated into blind holes. Ideally, the electrical resistance for identically designed nets should be single-valued. In practice, vias fabricated by high quality processes exhibit small variations about the nominal resistance value.

Figure 3 shows via net resistance plotted versus hole/land size from the boards supplied by one of the fabricators in this study. The data are displayed as notched box plots, with the median resistance centered on the notch and the box extending from the 25th to 75th percentile. Outside values plotted as individual dots extend beyond the upper adjacent values for each of the four nets. The spread in the resistance values is greater than desired for a high-quality process, and the presence of outside values can be an indication of potential reliability problems. The net with 6-mil holes and 14-mil lands had 12 data points greater than 1,500 milliohms with a maximum of 7,415 milliohms, while the net with 6-mil holes and 12-mil lands had 14 points above 1,500 milliohms, extending to a maximum of 11,367 milliohms. Further, the outside values in the nets with 6-mil holes dramatically impacted the resistance coefficient of variation, a relative measure of the spread in the data, and defined as 100 multiplied by the standard deviation divided by the mean. The coefficients of variation in this set of panels were 5.75, 5.92, 49.35, and 61.67 percent for the 8/16, 8/14, 6/14, and 6/12 hole/land combinations, respectively.

Summary

The concepts of capability and quality in the manufacture of vias have been introduced. Capability implies a manufacturing process that can consistently fabricate vias at low defect levels so that reasonably high yields may be attained. The Poisson model used to establish defect density and predict yield for vias shows that product yield drops significantly with increased defect density and increased numbers of vias per circuit board. Poor capability leads to increased scrap – resulting in greater costs, and potentially delaying deliveries.

Precision resistance measurements from via daisy chains are an indication of the quality of the vias and the processes used in their manufacture. Small resistance changes are to be expected in a high-quality, well-controlled via fabrication process. Large variations in the resistance of the via daisy chains indicate a process lacking control. The resistance coefficient of variation is one measure of quality, with values less than five percent indicating reasonably good control.

In the next column, data from a supplier management program will present a wide range of capability and quality among printed circuit suppliers. The last column in this three-part series will show that both capability and quality are essential elements of the fabrication process that must be achieved prior to proceeding with long-term reliability studies.

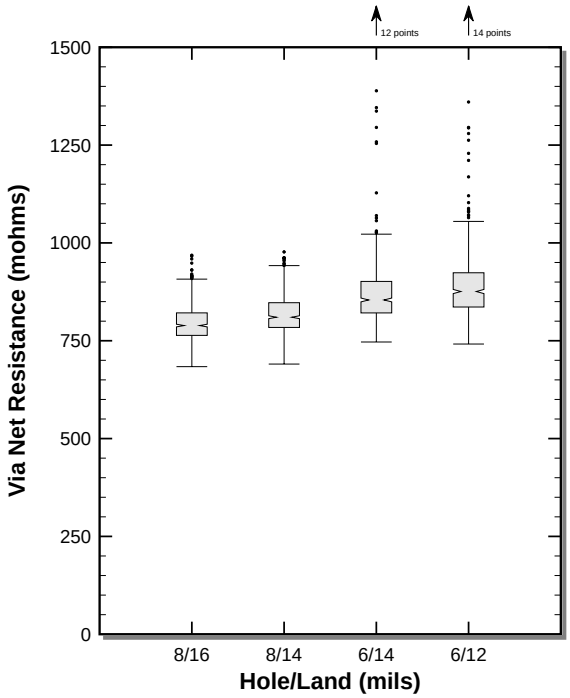

Figure 3. Microvia Quality – Two Layers Deep

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume V • Issue 11**

VIA CAPABILITY AND QUALITY RESULTS

The last column introduced the concepts of capability and quality in the manufacture of vias in printed circuit boards. This column presents the results of a supplier management program that included nine manufacturers. Data from through vias, and blind vias formed in two- and four-mil-thick dielectric emphasize the difficulty of fabricating blind vias, and show a wide range of capability and quality present in the industry. Next month's column will demonstrate that capability and quality must be achieved before initiating long-term reliability studies.

Supplier Management Study

Nine printed circuit board manufacturers fabricated forty 7.25" by 10.5" six-layer Process Capability Panels as participants in a supplier management program for an original equipment manufacturer. In addition to conductor and space modules and registration modules, four via-module designs were included in the panel. The via modules were included to collect quantitative data on capability and quality of through and blind vias.

Table 1 shows the parameters used in the four via module designs. The through via module combined 13.5- and 10-mil holes with 6-mil and 3-mil annular rings. The blind vias extending from layers 1-2 and 6-5 (one layer deep) had 6-, 5-, 4-, and 3-mil vias combined with 4-mil and 2-mil annular rings. These vias were formed through 2-mil-thick dielectric. The blind vias extending through 4-mil-thick dielectric from layers 1-3 and 6-4 (two layers deep) were 8- and 6-mils in diameter with 4-mil and 3-mil annular rings.

Via Type	Layers	Hole/Land				Vias per Net
		Net 1	Net 2	Net 3	Net 4	
Through	1-6	13.5/25.5	13.5/19.5	10/22	10/16	90
Blind	1-2,6-5	6/14	6/10	5/13	5/9	78
Blind	1-2,6-5	4/12	4/8	3/11	3/7	78
Blind	1-3,6-4	8/16	8/14	6/14	6/12	78

Table 1. Via Module Design Parameters

Each of the nine participating suppliers fabricated 129,600 through vias, 474,240 one-layer-deep vias, and 224,640 two-layer-deep vias.

Results

The results are summarized in Figures 1-3 for through vias, one-deep vias, and two-deep vias, respectively. Each graph has the resistance coefficient of variation plotted versus via defect density. Because of the range in the data, both axes are plotted as log scales. Low defect density and low coefficient of variation are desired in a well-controlled, high-quality via fabrication process. This region is at the lower left corner of each of the graphs. The shaded area contains data with the coefficient of variation below 5 percent and defect density less than 50 defects per million vias. In contrast, data in the upper right corner of the graphs is from the poorest-performing processes, with very high coefficient of variation and large defect density. The symbols in each figure decrease in size and become darker as the feature sizes become more difficult to manufacture.

Figure 1 is a graph of through via capability and quality. In all cases, defect levels were below 75 defects per million vias and the coefficient of variation below 8.1 percent. Most fabricators provided panels without defects and coefficients of variation ranging from two to six percent. One supplier recorded particularly good results, with zero defects[‡] and coefficients of variation below one percent for each of the four hole/land designs in the module.

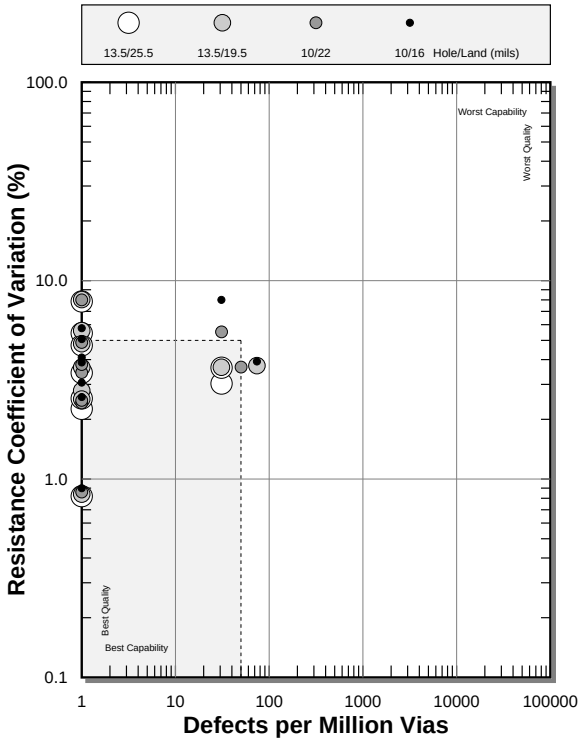

Figure 1. Through Via Capability and Quality

Blind vias are much more difficult to manufacture than through vias. Figure 2 shows results for the blind vias extending from the outerlayers to the first innerlayer (one layer deep). The data reported is from two different via modules, each with blind vias from layers 1-2 and 6-5. The larger circles are associated with larger hole/land combinations, and consequently are easier to fabricate. The data reflects this premise, with smaller circles generally having greater defect density and higher coefficients of variation. In this case, most of the data falls outside the shaded area with a good portion above 10 percent coefficient of variation and/or greater than 100 defects per million vias. However, one supplier (the same supplier that excelled in through-hole fabrication) performed much better than the others, with coefficients of variation ranging from 2.9 percent to 4.8 percent and low defect levels.

[‡] For convenience, zero defects are plotted at 1 defect per million vias.

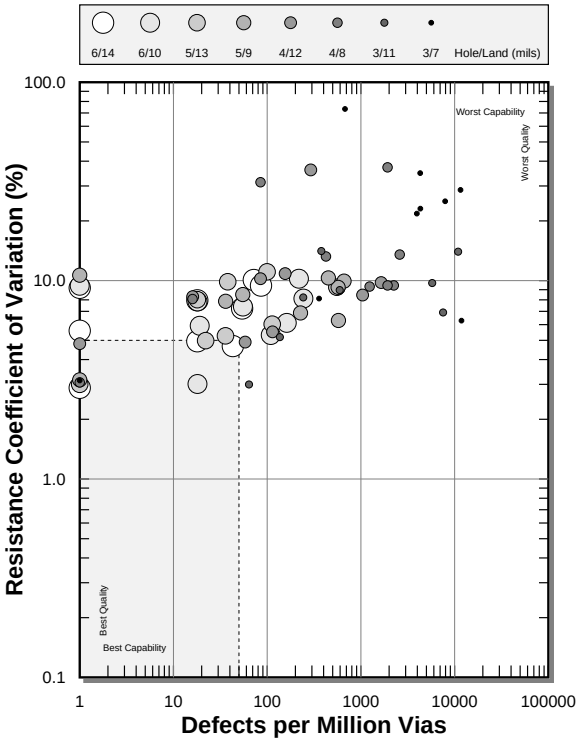

Figure 2. Microvia Capability and Quality – One Layer Deep

Blind vias extending from the outerlayer to the second innerlayer are even more difficult to manufacture. These results, shown in Figure 3, extend to 80 percent coefficient of variation and 64,000 defects per million vias. Once again, the supplier that performed best in the fabrication of through vias and one-layer-deep vias excelled in the fabrication of two-layer-deep vias, recording coefficients of variation below three percent and no defects for all four daisy chain nets.

Summary

Low via defect density is required to achieve acceptable yields, while controlled processes are necessary to fabricate high quality vias. Blind vias appear to be particularly difficult to fabricate, with metallization of the blind holes perhaps the most challenging part of the process.

Capability and quality varied significantly among the nine printed circuit board manufacturers participating in this supplier management program. For through vias, defect densities ranged from 0 to 75 defects per million vias, and resistance coefficients of variation ranged from 0.82 to 8.1 percent. Results for blind microvias formed in 2-mil-thick dielectric were worse, with defect densities ranging from 0 to 11,800 defects per million vias, and coefficients of variation ranging from 2.9 to over 75 percent. Vias formed in 4-mil-thick dielectric exhibited a further decline in quality, with coefficients of variation ranging from 2.6 to 80 percent, and defect densities ranging from 0 to 64,000 defects per million vias.

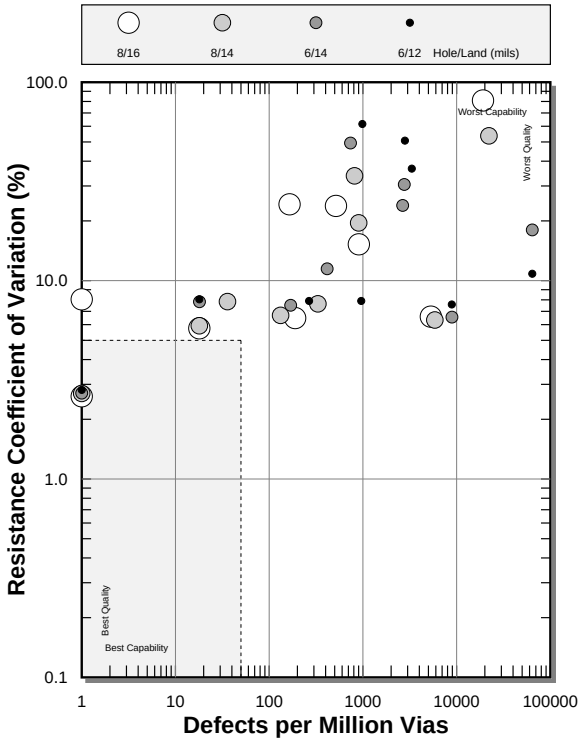

Figure 3. Microvia Capability and Quality – Two Layers Deep

While most suppliers recorded good results in through-via fabrication, only one of the nine suppliers demonstrated excellent capability and quality to manufacture both through vias and blind microvias formed in 2- and 4-mil thick dielectric.

Next month's column will show that both capability and quality are essential elements of the via fabrication process that must be achieved prior to running long-term reliability studies.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume V • Issue 12**

VIA CAPABILITY AND QUALITY FIRST … THEN RELIABILITY

The last column reported results from nine manufacturers that participated in a supplier management procedure. Results from through vias, and blind vias formed in 2- and 4-mil-thick dielectric emphasized the difficulty of fabricating blind vias, and displayed a wide range in capability and quality present in the industry. This column highlights the need to achieve capability and quality before beginning reliability studies.

Process Characterization

The data were collected from two process capability panels with 36 via modules on each side having 3-, 4-, 5-, and 6-mil diameter blind vias formed in 3.5-mil-thick dielectric between the outerlayers and the first innerlayers. There were 170 vias in each daisy chain net with a total of 48,960 vias per panel.

Figure 1 shows the range of resistances measured from microvia daisy chains. Significant variation was observed among the nets within the 3-, 4-, and 5-mil microvias, while a single outside value was observed in the more tightly controlled 6-mil data.

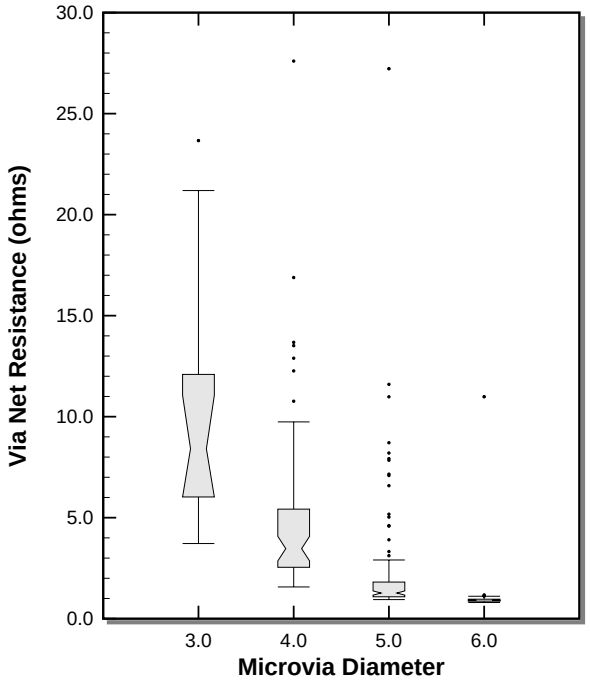

Figure 1. Microvia Resistance Range

Table 1 shows the number of good nets, along with the minimum, median, and maximum resistance value measured for each of the four via sizes. A "good" net is defined as one that is not "open" and not "shorted" to a neighboring net. All 144 of the 6-mil diameter daisy chains were good, while opens accounted for the reduction of nets in the chains with 3-, 4-, and 5-mil microvias. Also included in the table is the resistance coefficient of variation for each via diameter. The reduced population for the 3-mil microvias contributed to the smaller coefficient of variation recorded in this set.

The resistance cumulative distribution graph, shown in Figure 2, provides additional insight about the data. The 6-mil diameter microvias, indicated by the hexagons in the figure, appear to be normally distributed and well controlled except for a single point, accounting for the maximum value of 10.99 ohms. Neglecting this single outlier, 143 of the 144 nets ranged between 0.80 and 1.18 ohms. The data for the 5-, 4-, and 3-mil-diameter microvias, indicated by the pentagons, squares, and triangles, respectively, exhibited progressively worse resistance precision.

Microvia Diameter	Number of Nets	Measured Resistance (Ohms)			CoV (%)
		Minimum	Median	Maximum	
3.0	13	3.72	8.41	23.67	56
4.0	55	1.57	3.47	47.64	125
5.0	122	0.95	1.27	27.22	136
6.0	144	0.80	0.91	10.99	85

Table 1. Microvia Resistance Statistics

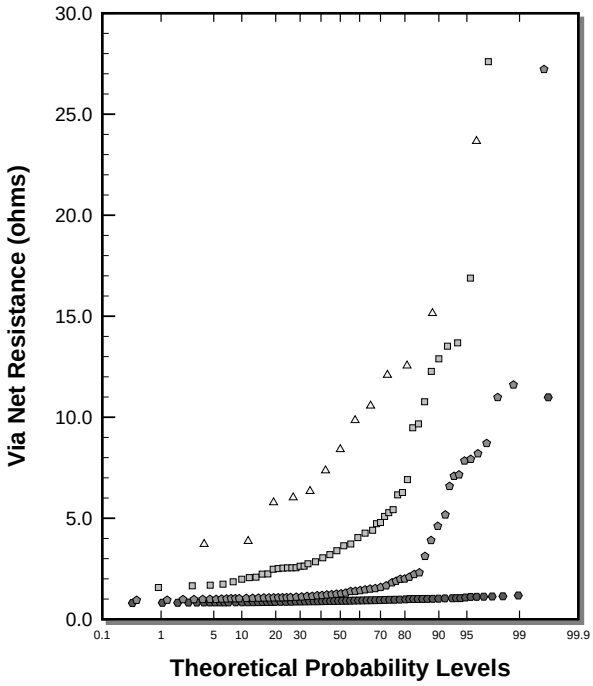

Figure 2. Resistance Cumulative Distribution

Assembly Simulation

Upon subjecting the process capability panels to two passes through an infrared reflow oven to simulate an assembly operation, the resistance of the daisy chain nets increased. Figure 3 is a graph showing the daisy chain resistance after stress plotted versus the resistance before stress. The solid diagonal line in the figure corresponds to no change in resistance, while the dashed line is plotted at a level where the resistance doubled. Triangles, squares, pentagons, and hexagons represent the 3-, 4-, 5-, and 6-mil microvias, respectively. Clearly, this thermal stress had a strong impact on the daisy chain nets, causing 4, 23, 19, and 2 additional opens to occur in the 3-, 4-, 5-, and 6-mil-diameter microvia nets, respectively.

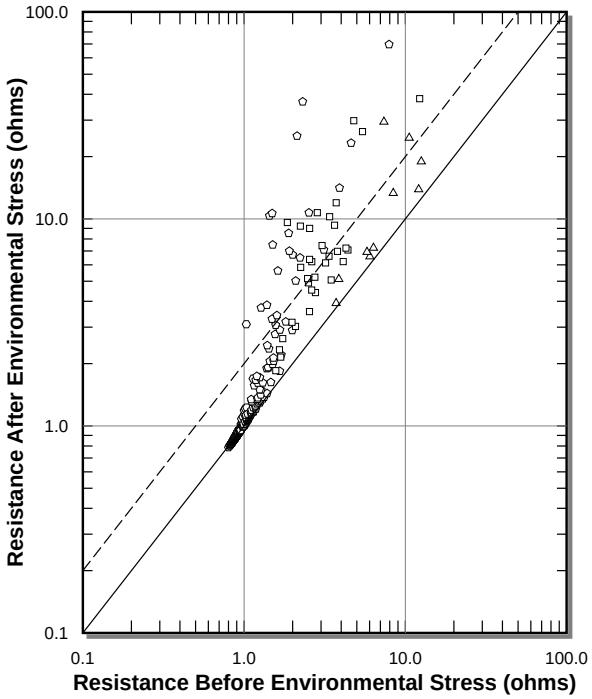

Figure 3. Changes in Resistance Due to Stress

Reliability

Both capability and quality must be satisfied before initiating reliability studies. If capability is marginal, defect levels will be too high to achieve acceptable process yields, or the presence of marginal interconnections will cause failures to occur. Precision resistance measurements from via daisy-chain nets can establish the quality of the microvias and the process used in their manufacture. A well controlled manufacturing process will form vias with low resistance coefficients of variation.

Figure 4 shows the precision resistance data collected from daisy chain nets with 4-mil-diameter microvias and 8-mil-diameter pads formed in 2-mil-thick non-reinforced dielectric from 33 process capability panels. There are data from a total of 568 daisy chains with 78 microvias per net plotted in the figure. At a probability level of 99 percent, the resistance of the nets begins to increase, indicating potential problems in one percent of the data. Inspection and test techniques such as cross-sections and electrical tests that are commonly used in the industry are not likely to discover the problem. Suppose reliability samples were fabricated by this process and subjected to reliability studies. The sample set may or may not include representatives from the one percent exhibiting increased resistance, depending on probability and the number of samples.

If the reliability sample set includes some of the high resistance nets, they will likely fail. Conclusions drawn from the reliability study and subsequent failure analysis will indicate that the samples are unacceptable, and further development is necessary with changes required in materials and/or manufacturing processes. These are valid conclusions, but significant time and effort could have been avoided if the data in Figure 4 were available.

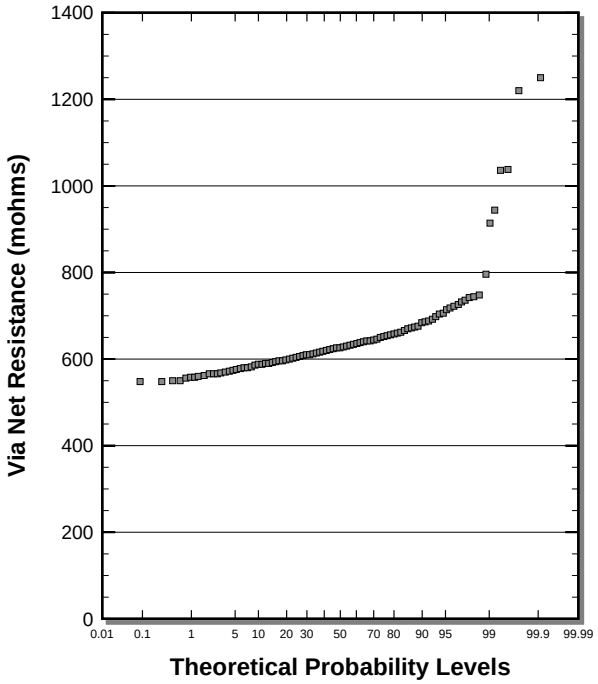

Figure 4. Resistance Cumulative Distribution of 4-Mil Microvias

On the other hand with only one percent of the population exhibiting higher-than-expected resistance values, there is a reasonable probability of excluding these marginal microvias in samples for reliability studies. Assuming the microvias with consistent resistance values were robust and passed the reliability tests, it is logical to conclude that the process is acceptable and product may be manufactured. Unfortunately, failures may occur during assembly or even worse in the field.

Conclusions

Precision resistance measurements acquired from microvia daisy chains provide quantitative data indicating process control – or the lack of control – associated with the materials and processes employed in their fabrication. Microvias manufactured by processes lacking control, indicated by a large range in resistance and large coefficients of variation, experienced increased resistance and a propensity to fail from exposure to the stress of an assembly simulation process.

While controlled manufacturing processes are not sufficient to guarantee reliability, they are essential prior to beginning reliability studies. Proceeding with reliability studies without knowing whether the manufacturing process is in control can lead to erroneous conclusions and very costly mistakes.

By characterizing microvia materials and manufacturing processes during their development and implementation, optimum processing parameters can be established that will lead to controlled processes. Measuring capability and quality using precision electrical resistance will confirm that processes are in control, and that subsequent reliability studies will be meaningful.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume V • Issue 2**

INVESTIGATING PROCESS CAPABILITY – PLATING

In the manufacture of printed circuits, the plating process provides metal deposition in holes that interconnects conductive traces formed on planes. Successful interconnection depends upon the combined quality of the preclean, photoresist application, imaging, developing, etching, drilling, and plating processes. More often than not, defects that begin in earlier steps are carried on to subsequent steps. This leads to low quality, questionable reliability, and even nonfunctioning circuits.

With the push for miniaturization, new technologies developed to form high-aspect-ratio through-holes and blind mircovias place significant demands on plating processes. Blind via holes are especially arduous to metallize, due primarily to the difficulty of transporting fresh chemistry into the holes, and removing gaseous byproducts that form in the holes.

This column will discuss some aspects of metallization processes, and present results from daisy-chain patterns manufactured by a laser-drilled microvia process.

Metallization Processes

The buildup of metal in the holes often begins with electroless copper. The process may include a soap or conditioner to remove grease and oils, a mild copper etchant to expose the grain structure and activate the copper surface, a catalyst (often a palladium/tin colloid), an accelerator to remove excess tin, electroless copper, and perhaps a strike of electroplated copper. Following the copper strike of approximately 0.1 mils, the holes are electroplated to the desired thickness, usually from 0.5 to 1.0 mils.

Some manufacturers use a full-build electroless process, eliminating the need for electroplating. Although slower, this technique can provide improved thickness uniformity compared to electroplating.

Most formulations of electroless copper contain formaldehyde, a recognized carcinogen. Direct metallization technologies have been developed as alternatives to electroless copper, in order to eliminate environmental and health issues. Each direct metallization system adds a conductive layer to the dielectric surfaces, providing a base for subsequent electroplated copper. Palladium-, carbon- or graphite-, and conductive polymer-based systems have been marketed as alternatives to electroless copper.

Except in full-build processes, electroplated copper is added to the holes to complete the interconnection, and provide the current-carrying capability required of the application. Acid copper sulfate solutions with organic additives, which are commonly used in the industry, usually provide the necessary tensile strength, ductility, uniformity, and finish required for reliable interconnections.

Plating Equipment

While dip tanks have been used traditionally for electroless/electroplate applications, horizontal conveyorized equipment is gaining acceptance, especially in direct metallization technology applications. Unlike conveyorized systems, panels are held in racks and transferred from tank-to-tank by hoists in automated dip tank processes.

Chemical baths must be analyzed, and additions made to maintain acceptable performance. To improve plating quality and assist in mixing and fluid transfer, mechanical oscillation and air-sparging systems may be utilized. Heaters and temperature controllers are used to maintain desired temperatures of critical baths.

Plating is initiated by applying a potential between the multilayer panels (cathode) and the anodes in the presence of the plating solution. Cathode current density for conventional copper-plating baths ranges between 20 and 40 amperes per square foot, while high-speed plating baths may operate as high as 150 amperes per square foot. Improved plating uniformity may be achieved by reducing the current density, especially for small hole and fine line applications. Pulsed plating may also improve uniformity in high aspect ratio holes and blind mircovias.

Types of Defects

Many types of defects become apparent after the plating process; with some having seeds from earlier process steps. For example, if not removed, drill smear can cause separation between innerlayers and the plated barrel. Plating voids may result from inadequate hole-cleaning prior to the metallization process. Residues remaining on the pads at the bottom of blind microvias can hamper plating or preclude electrical connection.

The metallization process itself can be responsible for defects as well. Thin or brittle copper can cause corner cracks and barrel cracks in plated-through holes. The inability to transport fresh chemistry to the surfaces, or to remove gas bubbles trapped in holes can lead to plating voids, especially in blind microvias.

Additional defects can occur during the patterning process. Loss of photoresist adhesion can lead to voids in holes in tent-and-etch processes. Alternatively, when metal-etch resists are used, photoresist residues remaining after development can prevent the deposition of tin/lead, leading to voids and "opens" as well.

Test for Via Quality

By examining the electrical resistance of via daisy-chain nets, the capability and uniformity of the process is quantified and the quality of the process is indicated. In the following example, 72 one-inch-square modules, each with four daisy-chain nets, are distributed equally over the top and bottom sides of an 18" by 24" multilayer panel. The hole diameter, land diameter, and interconnecting track width for each of the

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four designs are listed in Table 1. Each net includes 170 laser-drilled microvias, creating the daisy chain from the outerlayer to the first innerlayer, separated by approximately 3.5 mils of non-reinforced dielectric.

Design Number	Hole Diameter (mils)	Land Diameter (mils)	Track Width (mils)
1	6.0	12.0	5.0
2	5.0	12.0	5.0
3	4.0	10.0	5.0
4	3.0	10.0	5.0

Table 1. Via Daisy-Chain Design Data

The yield results attributed to "opens" in daisy chains from twenty panels are summarized in Table 2. Over 240,000 vias from each design were tested in this study. Notice that the defect density, reported in defects per million vias, increases with decreased hole diameters.

Design Number	Number of Nets	Number of Opens	Net Yield (%)	Defect Density
1	1440	3	99.79	12
2	1440	6	99.58	25
3	1440	13	99.10	53
4	1440	82	94.30	345

Table 2. Via Net Yield Results

The precision resistance of the daisy-chain nets provides additional insight into the process. By design, each module is identical. The precision resistance from each of the four daisy-chain nets, while different from one another, should have the same value from module to module under perfect manufacturing conditions. The variation in resistance for each design is indicative of process capability and uniformity.

Table 3 illustrates the variation in resistance measured for each design. Results for Designs 1 and 2 were similar, having means of 965 and 966 milliohms, respectively. Design 2 recorded a slightly larger range, standard deviation, and coefficient of variation than Design 1. The smaller holes in Designs 3 and 4 caused the mean resistance to increase to 1063 and 1309 milliohms, respectively. The range for Design 3 doubled compared to Designs 1 and 2, while that of Design 4 increased eight-fold compared to Design 1. Clearly, designs 3 and 4 exhibit significant variation, recording coefficients of variation of 6.49 and 14.86 percent, respectively.

Design No.	No. of Nets	Mean Net Resistance (mohms)	Range in Resistance (mohms)	Standard Deviation (mohms)	Coefficient of Variation (%)
1	1437	965	400	51	5.28
2	1434	966	425	54	5.56
3	1426	1063	892	69	6.49
4	1357	1309	3216	195	14.86

Table 3. Via Net Resistance Results

Notched box plots and cumulative distribution graphs contrast the performance among the four designs. Figure 1 displays notched box plots of via net resistance plotted versus design number. The notch is centered at the median of the data, while the box extends from the first to the third quartile (termed the *interquartile range*) encompassing 50 percent of the data. Bars are drawn to the *lower* and *upper adjacent values*. The lower adjacent value is determined by the minimum of the data, or the first quartile minus 1.5 multiplied by the interquartile range, whichever is closest to the median. Similarly, the upper adjacent value is determined by the maximum of the data, or the third quartile plus 1.5 multiplied by the interquartile range, whichever is closest to the median. Data that falls beyond the adjacent values are termed *outside values*, and are plotted as dots.

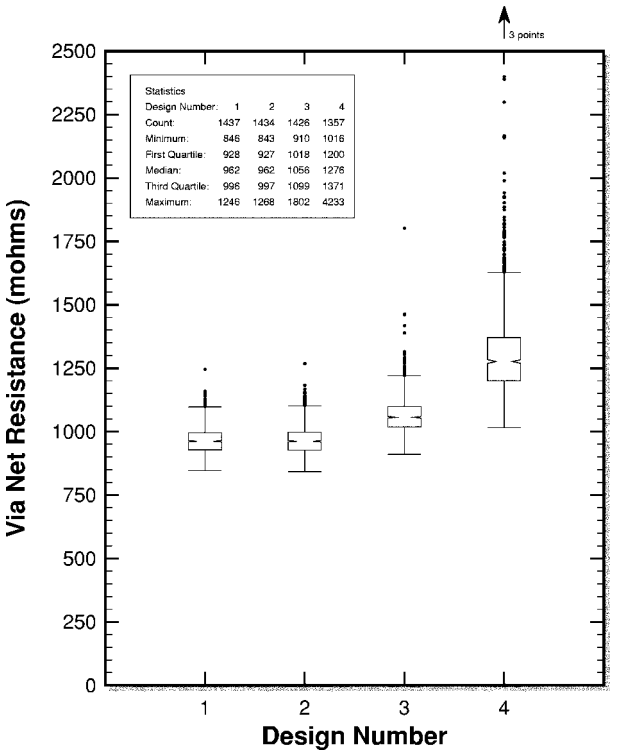

Figure 1. Via Net Resistance by Design Number

All four designs exhibit outside values greater than the upper adjacent value, but Design 3, and especially Design 4 show much greater variation than is acceptable in a viable

manufacturing process.

In Figure 2, via net resistance is plotted versus theoretical probability levels for each of the four designs. Normally-distributed data, when plotted in this fashion, form a straight line. The data from Designs 1 and 2 fall virtually on top of one another, and are nearly normally-distributed. Design 3 exhibits slightly greater resistance than Designs 1 and 2, with greater deviation from normal above the 99th percentile. Design 4 exhibits significant curvature above the 75th percentile, with the tail at the upper end extending well above the median. Once again, the data indicates that the larger holes provided higher quality and better uniformity than the smaller holes. The presence of high resistance values in the 3- and 4-mil diameter daisy-chain microvias suggests marginal interconnection and potential reliability issues that may lead to product failures.

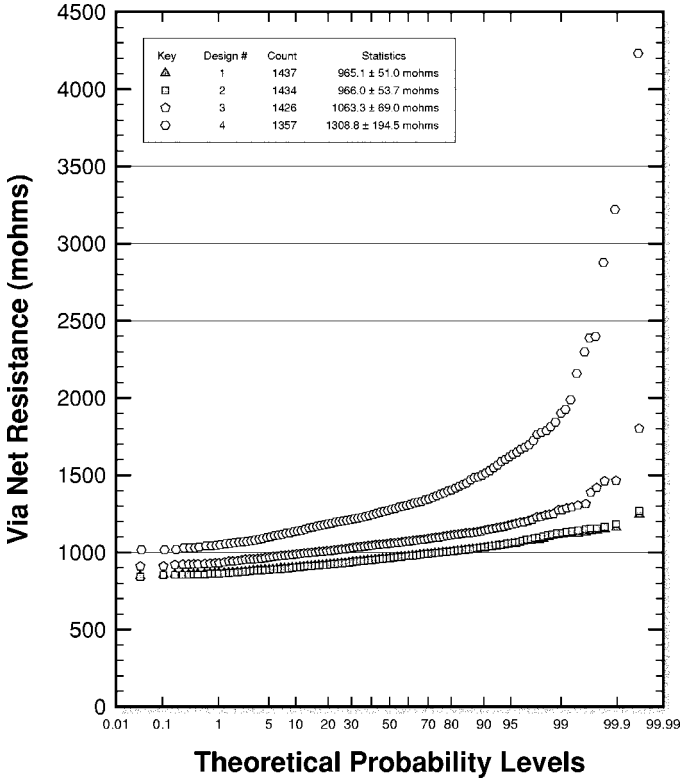

Figure 2. Resistance Cumulative Distribution by Design Number

Summary

Electroless copper deposition, followed by electroplated copper, is commonly used to complete interconnections in multilayer circuit boards. Some manufacturers use alternatives such as full-build electroless or direct metallization technologies. Regardless of the technology, each of the steps in the metallization process – such as cleaning, conditioning, micro-etch, activation, and deposition – must be completed successfully to provide quality interconnections.

High-aspect ratio through-holes and blind microvias utilized by high-density technologies place increased demands on plating processes. Even if the holes have been formed successfully and are properly cleaned, the challenge of completing the electrical interconnection by the plating process is complicated by the need to transport fresh chemistry into tiny microvias, while removing plating byproducts such as gas bubbles at the same time.

Sources of defects that cause "opens" in microvias, or those that pose threats to reliability must be identified and eliminated in high-quality manufacturing processes. Results from 20 multilayer panels illustrate that precision electrical resistance measured from microvia daisy-chain nets can provide quantitative data indicative of the capability and quality of the process used in their manufacture. The yield of the daisy-chain nets is used to calculate microvia defect density, while the distribution of precision resistance indicates the capability and uniformity of the process. Broad distributions in resistance, indicated by a large standard deviation, coefficient of variation, range, or high outside values, indicate marginal interconnections that may lead to reliability failures in products. Combined with designed experiments, the daisy-chain patterns, electrical test, and analysis techniques can help to identify the source of variation, and lead to solutions that improve capability and quality.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VI • Issue 1**

MICROVIA CAPABILITY, QUALITY, AND THE IMPACT OF REGISTRATION

Capability – the ability to fabricate microvias with sufficiently low defect density to achieve reasonable yields, and quality – the ability to form, metallize, and interconnect the microvias consistently with precision, have been the topics of the last three columns. Data was presented showing a wide range in capability and quality present among printed circuit board manufacturers, and provided evidence that both capability and quality are essential before meaningful reliability data can be collected.

This column examines the impact of registration on microvias. In particular, the ability to register microvias directly to their associated capture pads affects defect density and resistance coefficient of variation, which are measures of capability and quality, respectively.

Process Capability Panel

A six-layer 10.5 by 7.25 inch panel with 60 one-inch-square modules on each side was used in this study. The outerlayers were fabricated by a high density interconnect (HDI) process that formed blind vias from layers 1-2 and 6-5. Two registration modules and 38 microvia modules from each of 40 panels provided the data for the following discussion. The remaining modules included conductor patterns, through-via daisy chain and registration patterns, and via daisy chain and registration patterns extending from layers 1-3 and 6-4.

Registration Pattern

Figure 1 illustrates the registration module with seven columns of holes, each with a unique, designed clearance to corresponding bars formed on the first innerlayer. The four large pads at the bottom left of the figure are connected to the holes, while the four large pads at the upper left of the figure are connected to the copper bars formed on the innerlayer. By design, the holes are concentric with the "antipads" creating the clearance to the bars on the innerlayer. If registration is perfect, the clearance between the holes and the innerlayer bars will be maintained, and an "open circuit" will be measured for each test. Continuity measured between the holes and the bars patterned on the innerlayer indicates that a registration error equal to or greater than the designed clearance occurred.

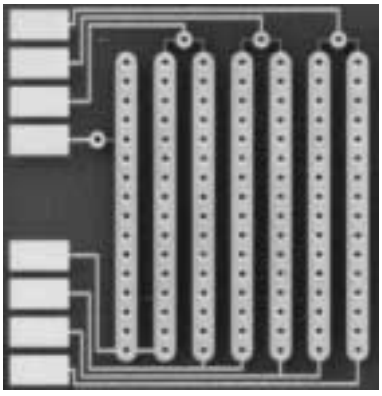

Figure 1. Registration Module

Figure 2 shows a schematic of a portion of the registration pattern along with the circuit analogue. In the registration schematic, circular openings (antipads) are formed in the copper bar. The hole at the top of the registration schematic is concentric with the antipad, and maintains clearance between the hole and the copper bar. The hole at the bottom of the registration schematic is shifted with respect to the antipad, and creates a "short" between the hole and the copper bar. The circuit analogue at the right of the figure shows a hole centered perfectly within the pad at the top, and a hole with breakout from the pad at the bottom.

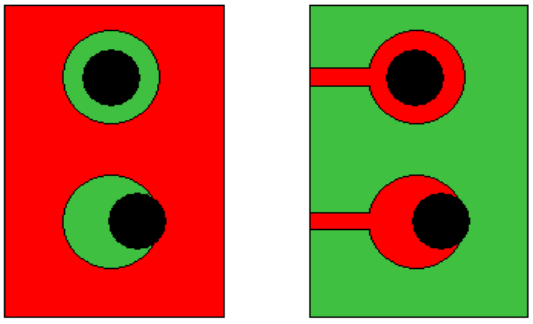

Figure 2. Registration Schematic and Circuit Analogue

The designed clearances in the registration pattern ranged from 1.0 to 6.0 mils in one-mil increments. The seventh clearance was -1.0 mils – intentionally designed to short. A total of 80 registration modules were fabricated.

Registration Results

Table 1 shows the registration results. The registration tests are converted to probability of breakout, and reported for each nominal clearance. Probability of breakout is defined at each clearance as 100 times the number shorted, divided by the total number of modules. The data shows that more than 50 percent of the modules had less than a one-mil registration error, while 2.0- and 4.0-mil clearances registered probabilities of breakout of 38.75 and 7.5 percent, respectively.

Design Number	Nominal Clearance (mils)	Probability of Breakout (%)
1	1.0	48.75
2	2.0	38.75
3	3.0	18.75
4	4.0	7.50
5	5.0	1.25
6	6.0	1.25

Table 1. Registration Results

Microvia Pattern

The microvia module, illustrated in Figure 3, contains four independent daisy chains that traverse two layers: either layers 1-2 or layers 6-5. Each of the four daisy chains contains 78

blind microvias with a unique hole/land combination. Two different via module designs were necessary to provide the eight hole/land combinations evaluated in this study. 3.0-, 4.0-, 5.0-, and 6.0-mil diameter microvias were paired with either 2.0-or 4.0-mil annular rings. The analysis includes more than 470,000 microvias fabricated on the 40 panels for this study.

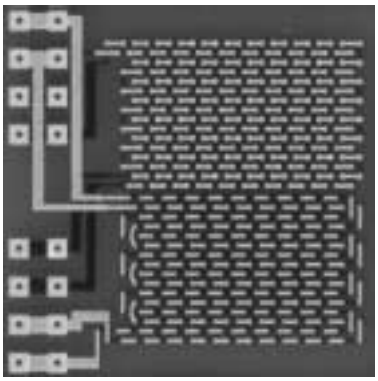

Figure 3. Microvia Module

Microvia Results

The quality of the microvias is established by the coefficient of variation of the resistance of the daisy chain nets, while the capability of the process used in their fabrication is determined by defect density. Table 2 shows capability results for each hole/land combination investigated. Defect density, reported in defects per million vias (DMV), increased with decreased hole diameter and smaller annular ring.

Hole Diameter (mils)	Land Diameter (mils)	Annular Ring (mils)	Microvia Defect Density (DMV)
6.0	14.0	4.0	18
6.0	10.0	2.0	162
5.0	13.0	4.0	36
5.0	9.0	2.0	660
4.0	12.0	4.0	114
4.0	8.0	2.0	1925
3.0	11.0	4.0	596
3.0	7.0	2.0	4301

Table 2. Microvia Capability

The impact of registration on capability is shown in Figure 4 where via defect density is plotted against microvia diameter. The square symbols are data from daisy chains with 4.0-mil annular rings, while the triangles are data from daisy chains with 2.0-mil annular rings. Established from registration results discussed earlier, the probability of breakout is reported for 2.0-and 4.0-mil annular rings at 38.75 and 7.5 percent, respectively. The curves drawn through the data are included to highlight the distinction between 2.0-and 4.0-mil annular rings. They are fit to the data and have the form:

$$y=ax^{-b} \quad (1)$$

with *a* and *b* positive constants. A shift toward increased defect density is observed with increased breakout probability for each microvia size. The results emphasize the need to improve registration accuracy and precision to take full advantage of HDI technologies.

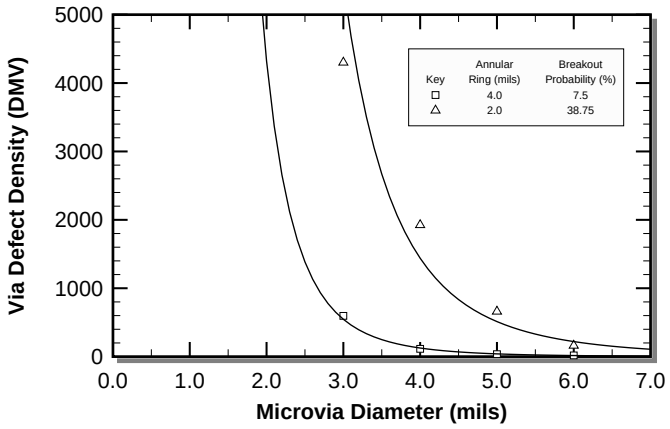

Figure 4. Capability versus Microvia Diameter

The quality of the microvias is summarized in Table 3, which reports the resistance coefficient of variation, defined as 100 times the standard deviation divided by the mean for each hole/land combination. The results confirm that smaller features are indeed more difficult to manufacture than larger ones. Quality decreased as hole diameters and annular ring dimensions decreased.

Hole Diameter (mils)	Land Diameter (mils)	Annular Ring (mils)	Resistance Coefficient of Variation (%)
6.0	14.0	4.0	4.95
6.0	10.0	2.0	6.13
5.0	13.0	4.0	5.27
5.0	9.0	2.0	9.94
4.0	12.0	4.0	5.52
4.0	8.0	2.0	37.21
3.0	11.0	4.0	8.95
3.0	7.0	2.0	34.81

Table 3. Microvia Quality

The impact of registration on the quality of microvias is illustrated in Figure 5. The coefficient of variation for the resistance of the microvia daisy chains is plotted against microvia diameter for 2.0-mil annular rings (triangles) with 38.75 percent probability of breakout, and 4.0-mil annular rings (squares) with 7.5 percent probability of breakout. The curves in the figure are fit to the data, and have the form of Equation 1. Clearly, the quality of the microvias degraded considerably with increased probability of breakout.

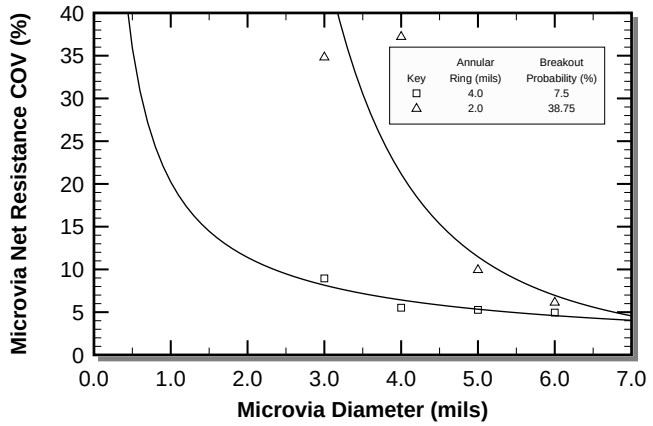

Figure 5. Quality versus Microvia Diameter

Summary

HDI employs narrow lines and spaces, and blind microvias to provide increased interconnection density. Hole diameters are limited by the dielectric material properties and thickness, the microvia formation and cleaning processes, the metallization process, and the pattern process. Land diameters must accommodate the microvia diameter with allowance for registration errors. Therefore, successful implementation of processes capable of smaller microvias and tighter registration will lead to increased interconnection densities.

Results from 40 process capability panels with registration and microvia patterns linked the formation and interconnection of microvias to registration performance. The study shows that breakout limits capability and degrades quality. As the microvia diameters decrease in size, the degradation in capability and quality due to registration is amplified. The data suggest that breakout should not be accepted.

The results remind us that registration is an important factor that can inhibit circuit miniaturization. Inadequate registration capability prevents the designer from selecting smaller lands. Further, it can lead to low yields and poor quality – two factors that can prove costly to printed circuit board manufacturers and their customers, original equipment manufacturers.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VI • Issue 2**

FABRICATOR SURVEYS – DO THEY TELL THE COMPLETE STORY?

Rules used by printed circuit board designers determine the density and performance that can be realized in finished products. The push toward miniaturization and performance improvements has increased the demand for blind microvias and the associated high density interconnect (HDI) technologies used in their manufacture. Tradeoffs available to designers in terms of feature sizes, stack-up, and layer count provide some flexibility to complete the design. The set of design rules selected for a particular design can have an enormous impact on the manufacturability of the printed circuit boards.

When technology roadmaps indicate changes in the existing design rules are necessary to accommodate new circuit designs, original equipment manufacturers (OEMs) may decide to survey their suppliers to ensure a smooth transition toward the new – and usually more difficult to fabricate – circuit boards. Unforeseen problems can lead to low yields, poor quality, and costly delays in delivery that can cause OEMs to miss market windows. Typical surveys may include a face-to-face session between the OEM and fabricator, a walk-through of the production facility, and an audit of the materials, equipment, and processes used by the fabricator to manufacture circuit boards. However, capability claims made by fabricators may not meet the OEM's expectations.

This column presents an example of one OEM who avoided substantial costs in terms of quality and delivery delays by collecting quantitative data on manufacturing capability and quality following the survey. As a result of the study, design rules were changed to improve the manufacturability of the circuit boards. Further, participating fabricators collected quantitative data showing weaknesses in their processes, and directions for improvement.

Technology Roadmap

The technology roadmap of the OEM for 1998 included the following features formed on large 24-layer multilayer boards that were 0.124 inches thick: 4-mil lines and spaces on innerlayers, 5-mil lines and spaces on outerlayers, 13.5-mil (drilled) diameter through vias, 5-mil diameter blind microvias with 12-mil diameter pads (one layer deep), and 7-mil diameter blind vias with 14-mil diameter pads (two layers deep). In face-to-face discussions with three key suppliers, the OEM was assured that these design rules could be achieved in their products.

Because many of these features had not been used in previous designs, the OEM was concerned that poor yield could cause delays in delivery, especially when ramping up to full production quantities. Further, inadequate control of feature sizes would lead to poor quality that could jeopardize performance and reliability. To address these concerns before releasing new designs to manufacture, the OEM decided to have the suppliers fabricate process capability panels (PCPs) designed to measure manufacturing capability and quality.

Process Capability Panel

A 24-layer process capability panel was designed to study manufacturing capability and quality. The 16 by 22-inch active area of the 18 by 24-inch PCP was covered with conductor and space, via, and registration features. The feature sizes (reported in mils) that were incorporated into the design are summarized in Tables 1-5. In addition to the OEM roadmap features for which the suppliers claimed capability, smaller, more difficult-to-manufacturer features were included to determine the "knee of the curve" in terms of capability.

Layer	[Conductors] Spaces
Outerlayers	[4] 4 [5] 5 [6] 6 [7]
Internal Signal Layers	[3] 3 [4] 4 [5] 5 [6]

Table 1. PCP Conductor and Space Features

Layer	Designed Clearances
Internal Signal Layers	2, 3, 4, 5, 6, 7, 8
Internal Plane Layers	2, 3, 4, 5, 6, 7, 8
One Deep Blind Vias	1, 2, 3, 4, 5, 6, 7
Two Deep Blind Vias	1, 2, 3, 4, 5, 6, 7

Table 2. PCP Registration Features

Feature	Net #1	Net #2	Net #3	Net #4
Via Diameter	13.5	13.5	10	10
Land Diameter	28	23	25	20

Table 3. PCP Through Via Features

Feature	Net #1	Net #2	Net #3	Net #4
Via Diameter	6	5	4	3
Land Diameter	12	12	10	10

Table 4. PCP One-Deep Microvia Features

Feature	Net #1	Net #2	Net #3	Net #4
Via Diameter	8	7	6	5
Land Diameter	14	14	12	12

Table 5. PCP Two-Deep Via Features

Test Results

The results from process capability panels submitted by three suppliers failed to meet expectations of the OEM in several respects. Figures 1 and 2 show conductor and space defect density for outerlayers and innerlayers, respectively, averaged over the three suppliers. High defect levels indicate poor manufacturing capability, moderate defect levels indicate that added costs of rework and repair will be required, while low defect levels indicate that reasonable yield with minimal

rework and repair will be achieved.

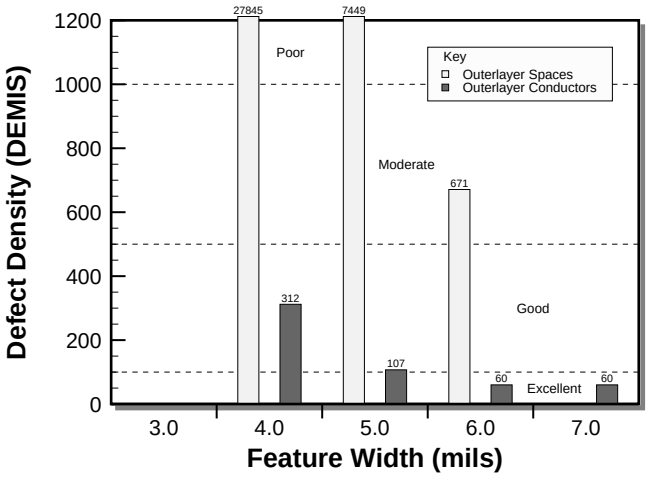

Figure 1. Average Outerlayer Conductor & Space Defect Density

Defect densities below 100 defects per million inches (DEMIS) are indicated as excellent performance in the figures, while 100 to 500 DEMIS is good, 500 to 1000 is moderate, and above 1000 is poor.

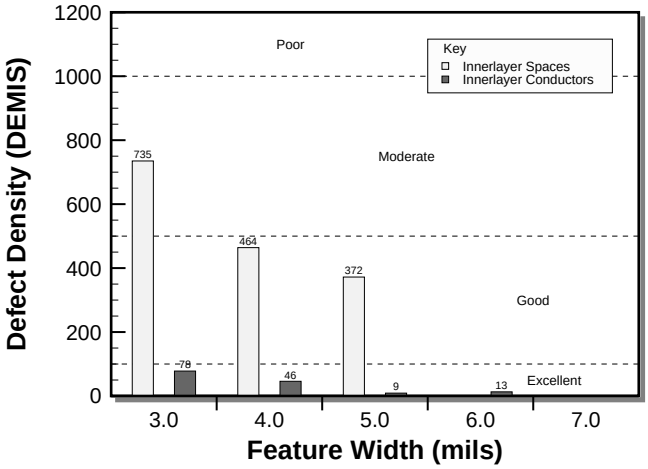

Figure 2. Average Innerlayer Conductor & Space Defect Density

The data show that "shorts" in narrow spaces between conductors is the overriding cause of failures. Defect density is much greater on outerlayer features (the latter part of the process when the panels have substantial investment in terms of time and materials) than on corresponding innerlayer features. Further, defect densities generally increase with decreased feature widths.

Through-via registration capability fell short of expectations as well. Figure 3 shows probability of breakout versus annular ring for signal-layer registration, averaged over the three participating suppliers. Performance below 5 percent breakout probability was considered excellent; 5 to 15 percent, and 15 to 25 percent was rated good and moderate, respectively; and above 25 percent was considered poor. The results indicate that larger diameter lands (perhaps with teardrops) are necessary to preclude breakout – a requirement that will have a significant impact on routing density.

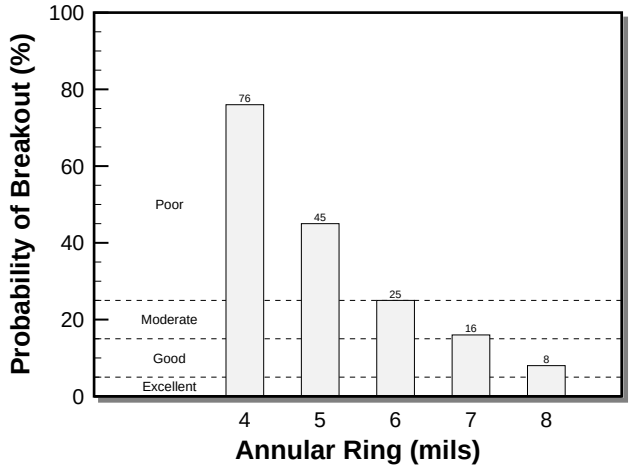

Figure 3. Average Through Via Registration

Registration results for one-deep blind microvias, shown in Figure 4, were better than through via registration but below expectations. To avoid breakout, the data shows that larger-than-expected lands must be used with microvias, placing additional routing constraints on designers.

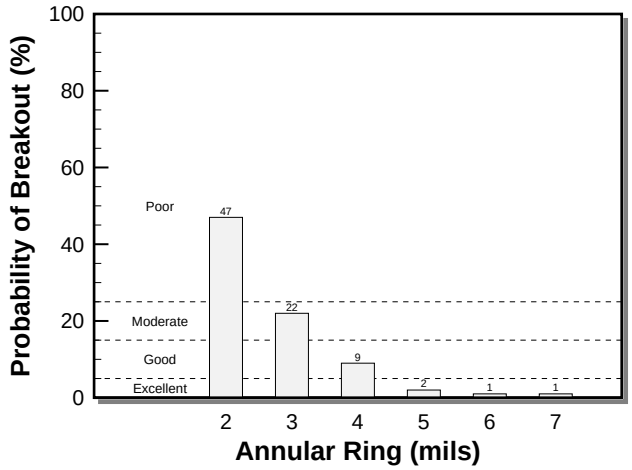

Figure 4. Average One-Deep Microvia Registration

The capability results for through vias, one-deep microvias, and two-deep vias are shown in Figures 5, 6, and 7, respectively. Defect density due to "opens" in daisy-chain nets, averaged over the three participating suppliers, is plotted for each via/land combination in the process capability panel. Defect densities below 50 defects per million vias (DMV) indicate excellent performance in the figures. For ranges between 50 and 100 DMV, between 100 and 500 DMV, and

above 500 DMV, performances were rated good, moderate, and poor, respectively.

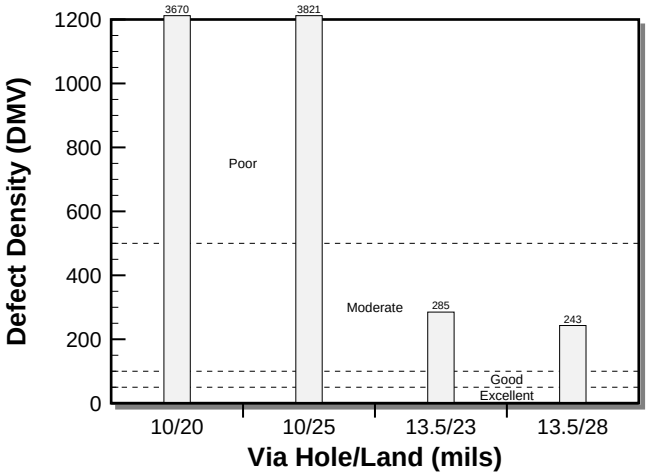

Figure 5. Average Through Via Defect Density

Average capability for 10-mil diameter through vias was poor, while 13.5-mil diameter through-via capability was moderate. A small improvement was observed when the 13.5-mil vias were combined with larger diameter lands.

Results for one-deep microvias are shown in Figure 6. Capability was directly related to microvia diameter, with average defect densities increasing as via diameters decreased. Six-mil diameter microvias recorded moderate capability, while smaller diameter microvias were all poor.

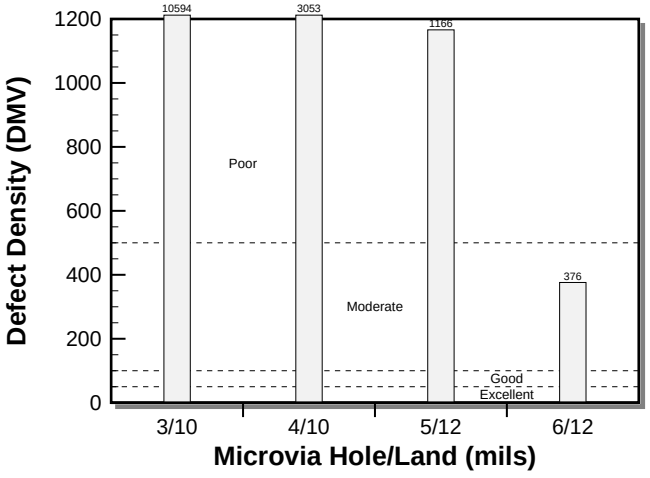

Figure 6. Average One-deep Microvia Defect Density

Two-deep vias proved the most difficult to manufacture (Figure 7), with unacceptable defect levels measured across all four via/land combinations. To successfully interconnect these higher aspect ratio vias, advancements in the formation, cleaning, metallization, and patterning processes are required.

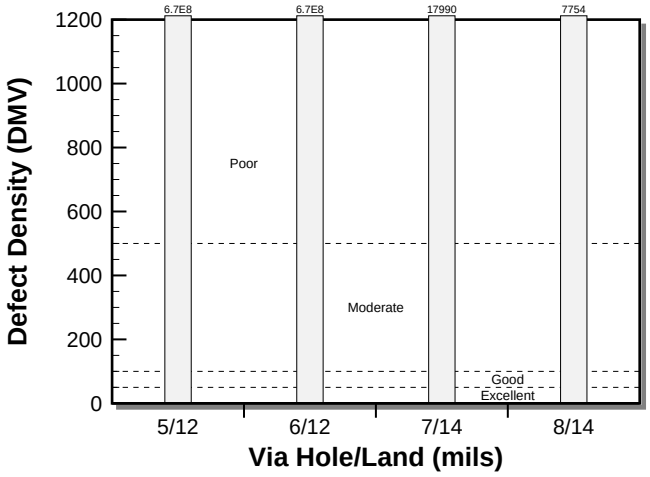

Figure 7. Average Two-deep Via Defect Density

Design-Rule Changes

Based upon the results from the three participating suppliers, the OEM made design-rule changes to lower risk, avoid manufacturing problems, improve quality, and ensure timely delivery of future designs. Table 6 shows the minimum feature sizes that were recommended based upon the supplier survey, and the changes resulting from the process capability panel tests.

Feature	Capability Indicated by Survey	Design Rule Changed To
Innerlayer line/space width	4/4	4/5
Outerlayer line/space width	5/5	5/6
Through vias/land	13.5/23	13.5/28
Blind vias/land (1 deep)	5/12	6/16
Blind vias/land (2 deep)	7/14	-

Table 6. Design-Rule Changes

The major design-rule changes include:

- Increase minimum space widths on both innerlayers and outerlayers.
- Narrow controlled-impedance traces must be placed on innerlayers.
- Use 13.5-mil or greater drill for through vias.
- Increase minimum annular ring to 6 mils for through vias.
- Increase minimum via/land to 6/16 for one-deep vias.
- Do not use 2-deep blind vias until improvements in capability are demonstrated.

Summary

While surveys of printed circuit board suppliers are necessary as part of the OEM supplier management process, they are not sufficient to establish and maintain a group of suppliers with

the capability and quality needed to ensure timely delivery of future designs. In the example presented, results from tests of process capability panels contradicted surveys of three key suppliers. The data collected from process capability panels were used by the OEM to redefine design rules, which improved the manufacturability, quality, and reliability of their products.

Collaboration between the OEM and the printed circuit board suppliers has been a winning experience for both teams. The printed circuit board suppliers have been very supportive of the effort, because they recognize that the revised design rules will provide higher yields and better quality when ramping up production on products using these features. Further, the OEM has encouraged the suppliers to address the weaknesses in their processes, and improve capability and quality. As a result of these efforts, recent tests show improved results for two-deep vias, with potential for them to be used in future designs.

Acknowledgments

CAT Inc. would like to thank David Evans of Teradyne Inc., Agoura Hills, CA, and Wayne King of Teradyne Inc., San Jose, CA, for their contributions to this column.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VI • Issue 4**

CONDUCTOR WIDTH IN DENSE AND SPARSE AREAS

Controlled impedance designs are commonly required for advanced, high frequency applications where signal timing and integrity are paramount. The characteristic impedance of a signal line depends upon material properties and geometric relationships of the finished circuit board. The dielectric constant, conductor width and height, and distances between signal traces and their respective ground plane(s) contribute to and affect the characteristic impedance of the circuit. Sophisticated design software is available to assist in establishing critical dimensions necessary to achieve the desired impedance, but achieving those dimensions in the finished circuit board can be a difficult assignment for the process engineer charged with the responsibility.

Finished conductors vary from their designed width primarily because of variations in local processing conditions. If factors such as the local temperature, chemistry, and flow conditions were precisely the same, then there would be no variation in conductor width over the surface of the panel, from side-to-side on panels, and from panel-to-panel, independent of the separation distance between conductors. The problems facing equipment designers and process engineers alike center on delivering bulk chemistries, by way of sumps, tubes, pumps, and nozzles, to panel surfaces so that local processing conditions are as uniform as possible.

Most process engineers in the printed circuit board industry would agree that isolated conductors – those with large spaces on either side – etch differently from those in dense circuit areas where spaces are narrow. It is intuitive that transporting materials into narrow spaces is more difficult than in areas with wide spaces, slowing the reaction rate and accounting for the disparity. It is not intuitive, however, how the design of the processing equipment and the equipment settings affect the width of finished conductors in dense and sparse regions on the circuit board. This column presents results from five etchers that exhibit significant differences in capability to control the width of narrow conductors, independent of space width.

Process Capability Panel

A printed circuit board process engineer investigated etcher performance prior to submitting an order for equipment purchase. The engineer was concerned with the uniformity that the etching process imparted on product, and the impact on width when conductors were distant from neighboring conductors compared to those that were in close proximity to one another.

To study the effects of etching on conductors in dense and sparse areas, a process capability panel was designed with two conductor module patterns: one with narrow spaces, and the other with wide spaces. The one-inch-square modules were arranged in 16 rows and 22 columns, covering the surface of an 18 by 24 inch panel. The modules with narrow spaces are shaded in Figure 1, while the modules with wide spaces are not shaded.

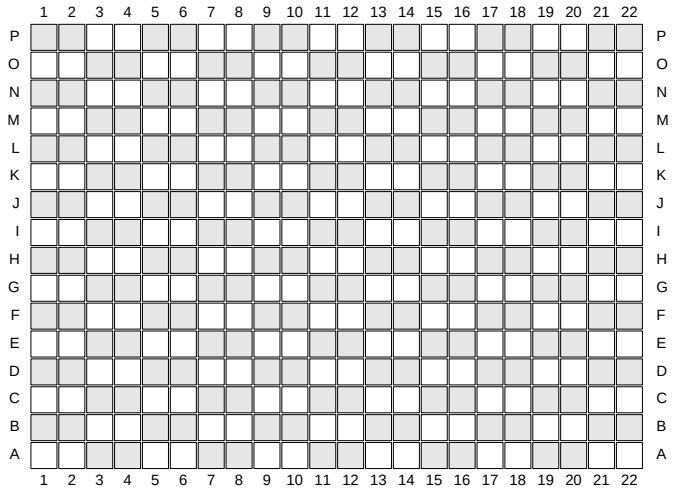

Figure 1. Process Capability Panel Schematic

Figure 2 shows four modules which correspond to those in positions A1, A2, B1, and B2 on the panel. The dense pattern had 4-, 5-, 6-, and 7-mil lines separated by 5-, 6-, and 7-mil spaces, respectively, while the sparse pattern incorporated the same conductor widths separated by 30-, 31-, and 32-mil spaces, respectively. As shown in Figure 2, there were horizontally- and vertically-oriented modules of the same type adjacent to one another. The horizontal/vertical orientation forms a checkerboard pattern over the panel area, while the dense/sparse modules were placed on the panel according to the shading in Figure 1.

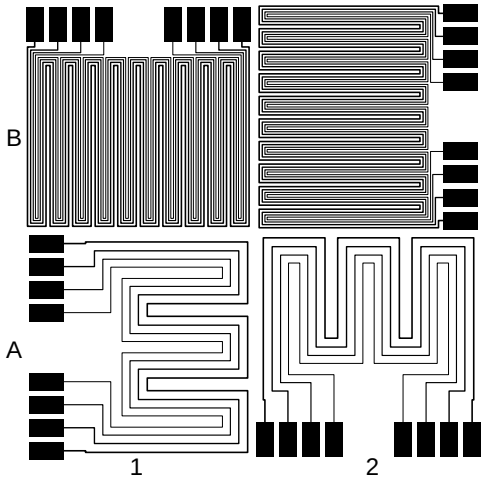

Figure 2. Dense and Sparse Conductor Modules

Procedures

Approximately 100 innerlayer panels were imaged and developed with the process capability panel pattern. "Top side" artwork, designated layer L1, was imaged facing up in the printer, while "bottom side" artwork, designated layer L2, was imaged facing down in the printer. These panels were randomized, and etched on five different etchers to study their

impact on conductor width uniformity. Some of the panels were processed with the "top side" up in the etcher, and some with the "top side" down in the etcher.

Results

Data from a small subset of the panels used in this study illustrates the concerns of the process engineer, and confirms that all equipment is not the same. Data from the "top side" artwork (layer L1) of ten panels, two from each etcher, is shown in Figure 3. Results from 352 modules on a single panel side that either faced up or faced down during the etching process are shown for each of the five etchers, designated A, B, C, D, and E, respectively. Conductor width difference is plotted as notched box plots for each panel side in the figure. Conductor width difference was calculated for pairs of diagonally adjacent modules by subtracting the width of the nominal 5-mil-wide conductor in sparse modules from width of the corresponding conductor in dense modules. Referring to Figure 2 for example, the width of the 5-mil conductor in module A2 was subtracted from the width of the 5-mil conductor in module B1, and the width of the 5-mil conductor in module A1 was subtracted the width of the 5-mil conductor in module B2. This procedure eliminates the horizontal/vertical bias that may be present by comparing horizontal sparse and dense modules to each other and vertical sparse and dense modules to each other. Further, spatially dependent variations are minimized by comparing results from modules that are close to one another.

In all cases, the median conductor width difference (located at the notch in the box plot diagram) was positive, indicating that most of the conductors in sparse modules were narrower than those in dense modules.

Results from etcher A show similar distributions for the two panel sides, one facing up and the other facing down during etching. The median conductor width difference for etcher A was 0.5 mils, with the greatest differences between sparse and dense areas on the order of 1 mil.

Etcher B exhibited the poorest performance, with some conductors in dense areas more than 1.5 mils wider than their counterparts in sparse areas on the side facing up during etching. Etcher B also recorded the greatest discrepancy between dense and sparse areas among the five etchers on the side facing down during etching.

Etcher E displayed good performance on the side facing down during etching, but poor performance on the side facing up.

The best performance was recorded by etcher D, having the smallest discrepancy between dense and sparse areas when considering panels processed up and down in the etching equipment. In all cases, discrepancy between dense and sparse areas for etcher D was within ± 0.6 mils, with the median difference between 0.1 and 0.2 mils.

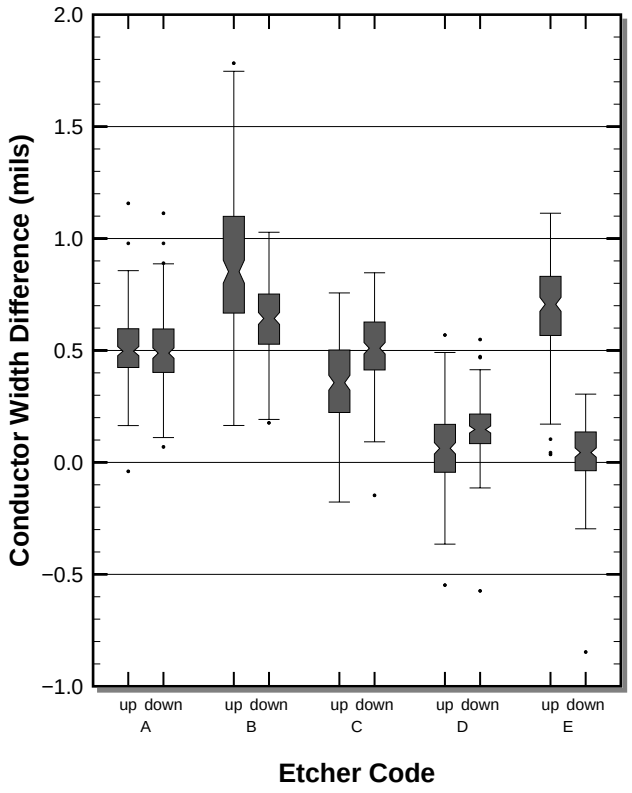

Figure 3. Conductor Width Difference Between Dense and Sparse Modules

Figure 4 shows a three-dimensional rendering of conductor width for the 5-mil-wide conductors formed on the panel that was processed facing up in etcher B. When compared to the schematic shown in Figure 1, the 5-mil lines from dense modules were wider than those from sparse modules, with the largest discrepancy occurring near the middle of the panel. This pattern, which had the greatest impact on conductors with narrow spaces, may be due to the phenomenon known as puddling, which causes reduced etching to occur in the middle of the panel compared to the perimeter.

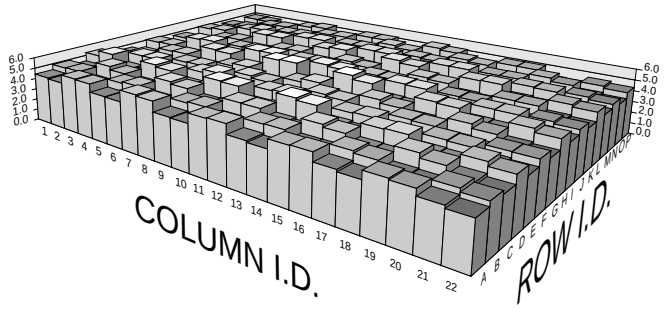

Figure 4. Conductor Width 3D Graph - Panel Facing Up in Etcher B

In contrast to the results from etcher B, Figure 5 displays conductor width for the 5-mil conductors formed on the panel that was processed facing up in etcher D. The uniformity in

this case is superior to that from etcher B, with noticeable differences between dense and sparse occurring in column 22, and minor differences elsewhere.

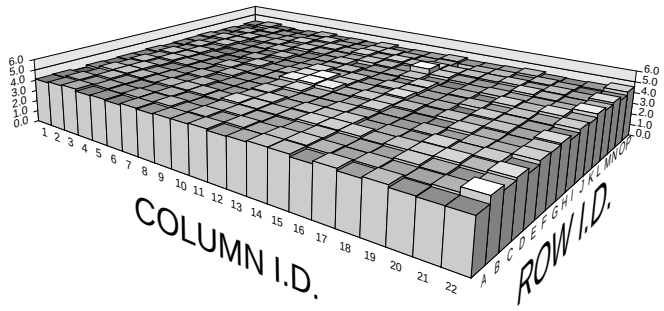

Figure 5. Conductor Width 3D Graph - Panel Facing Up in Etcher D

Summary

Modern high-speed electronic circuits, such as those used in computers and communications systems, require controlled impedance lines to maintain signal integrity. Conductor width is one of the parameters that affect the characteristic impedance of the circuit. Controlled impedance lines are often distant from neighboring conductors, while narrow lines and spaces are used in dense circuit areas to facilitate interconnection.

While it is necessary to form narrow lines in both dense and sparse areas on printed circuit boards, it is a difficult task to control the process so that their finished widths are the same. Both the etching equipment and the processing parameters can affect the uniformity of features between dense and sparse areas.

Results from five etchers showed significant differences in capability to consistently form narrow conductors in both dense and sparse areas. In the worst performance, nominal 5-mil-wide conductors were between 0.2 and 1.7 mils wider in dense areas than in sparse areas. In the best case, the discrepancy in conductor width between dense and sparse areas was within ± 0.6 mils, with the median offset of 0.1 to 0.2 mils.

Clearly, all etching equipment is not the same. Some equipment designs may have features that help to eliminate treatment differences between dense and sparse areas, while other designs may not. Prior to purchasing new etching equipment, it is prudent to investigate the performance of available systems to determine which systems can satisfy the demands required of new technology.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VI • Issue 5**

VIA CAPABILITY, QUALITY, AND RELIABILITY

In the last column, finished conductor width was discovered to be dependent upon the spacing between conductors. While conductors formed in sparse areas were generally narrower than those in dense areas, the degree of disparity between the two was linked to the processing equipment used in their manufacture.

Via fabrication is revisited in this column by Teradyne, Inc. to assess their suppliers' ability to manufacture vias in terms of capability, quality, and reliability. The technology investigated is high layer-count multilayer printed circuits, with high aspect ratio through vias, and one- and two-deep blind vias formed on both sides of the board. Design rules were relaxed in this second round of tests after significant problems were identified in fabricating one- and two-deep blind microvias in the first round. Even with relaxed design rules, however, two of the five fabricators participating in this study delivered samples having significantly lower capability, quality, and reliability than the other three.

Process Capability Panel

The process capability panel was an 18- by 24- by 0.125-inch design with 24 layers. Each panel had one-inch-square modules arranged in 16 rows and 22 columns. There were a total of 44 through via modules, 41 one-deep via modules, and 43 two-deep via modules per panel. In addition to via modules, there were outerlayer and innerlayer conductor modules, through via registration modules, one- and two-deep via registration modules, soldermask registration modules, and surface microstrip, embedded microstrip, and stripline controlled impedance modules.

Figure 1 shows an example of a blind via module, with the test pads at the left edge of the module. The precision resistance is measured for each of the four daisy-chain nets in the module by passing a known current through the net and measuring the voltage drop across the net. Known as a 4-wire or Kelvin measurement technique, this method eliminates the resistance of the leads from the meter to the pads.

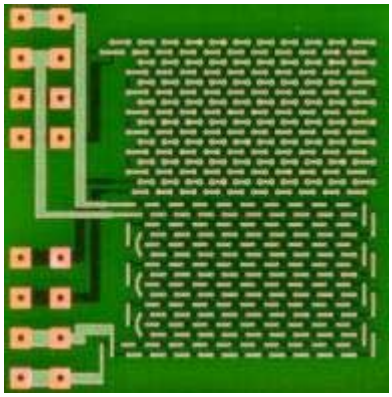

Figure 1. Example Blind Via Module

There were 11,968 through vias, 22,632 one-deep blind vias, and 23,736 two-deep blind vias in each process capability panel. Table 1 lists the via diameter, land diameter, dielectric thickness, and aspect ratio of the via for each of the four nets and three module types. The aspect ratios for the through vias ranged between 9.26 and 12.5, while the aspect ratios for the blind vias were less than 1.0 in all cases.

Type	Via Diameter (mils)	Land Diameter (mils)	Dielectric Thickness (mils)	Aspect Ratio (H/D)
Through Vias	10.0	22.0	125	12.50
	11.0	23.0	125	11.36
	12.0	24.0	125	10.42
	13.5	25.0	125	9.26
One-Deep Blind Vias	5.0	15.0	3.5	0.70
	6.0	16.0	3.5	0.58
	7.0	17.0	3.5	0.50
	8.0	18.0	3.5	0.44
Two-Deep Blind Vias	9.0	19.0	7.5	0.83
	10.0	20.0	7.5	0.75
	11.0	21.0	7.5	0.68
	12.0	22.0	7.5	0.63

Table 1. Via Details

Procedures

The process capability panels were manufactured by five fabricators. The completed panels were electrically tested prior to environmental stress by CAT Inc., and the data stored to disk for subsequent analysis. The Original Equipment Manufacturer subjected the panels to two passes through a forced hot air convection oven to simulate an assembly process, and the panels were re-tested by CAT Inc. to determine changes in resistance caused by the stress. Finally, the data was analyzed to establish the impact of stress on the vias.

Results

Via capability and quality have been used in previous columns to compare the performance among fabricators to manufacture vias. Figure 2 shows the results from the five fabricators prior to environmental stress. For each via diameter studied, the defect density (a measure of capability) is plotted on the X-axis in the figure, while resistance coefficient of variation (a measure of quality) is plotted on the Y-axis in the figure. Best performance is indicated in the lower left corner of the graph, and is represented by low defect density and low coefficient of variation, while the worst performance in indicated at the upper right corner of the graph, where defect density and coefficient of variation are high. The shaded region (bounded by dashed lines) contains results below 50 defects per million vias and coefficient of variation below five percent. The symbols depict the results from the five fabricators, A, C, D, E, and F. All results from fabricators A, C, and D bordered or were within the shaded region, while fabricators E and F had much poorer capability and quality, reflected by many points extending far outside of the shaded region.

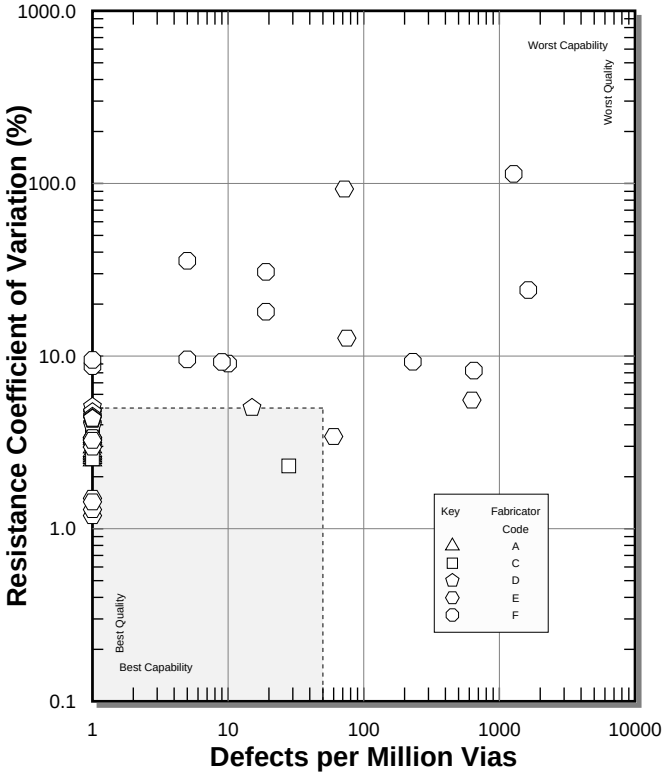

Figure 2. Via Capability & Quality Before Stress

While Figure 2 shows that overall performance before stress among the fabricators varied significantly, more detailed data on capability and quality is provided in Figures 3 and 4. For each of the five fabricators, Figure 3 shows via defect density in defects per million vias prior to stress plotted against each via diameter in the process capability panel. The 5-, 6-, 7-, and 8-mil diameter blind vias were one-layer deep, the 9-, 10-, 11-, and 12-mil diameter blind vias were two-layers deep, and the 10-, 11-, 12-, and 13.5-mil diameter vias extended through the board. All vias from fabricator A were defect-free, while fabricators C and D had low defect levels in 10-mil diameter through vias and 7-mil diameter blind vias, respectively, and no defects elsewhere. Fabricator E recorded high defect density in the 5-mil diameter vias, and moderate defect densities in the 6-, 7-, and 9-mil diameter vias. Having the poorest overall performance, fabricator F recorded zero or low defect densities in the blind vias, but moderate to high defect densities in the through vias.

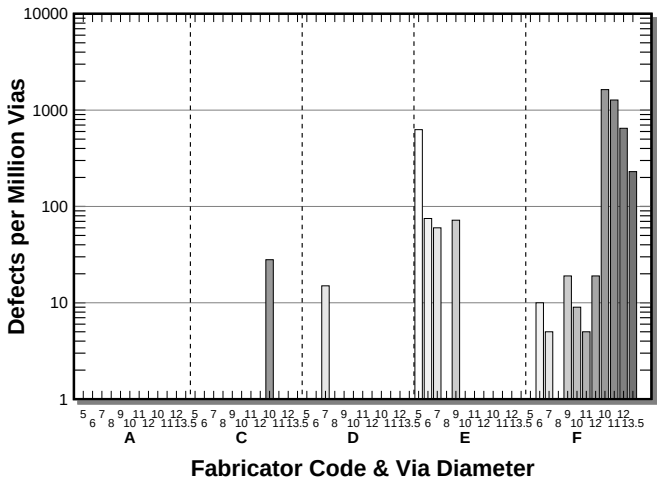

Figure 3. Via Capability Before Stress

Via quality before stress is shown in Figure 4. Defined as the standard deviation divided by the mean and expressed in percent, via net resistance coefficient of variation is plotted for each via size and fabricator. Fabricators A, C, and D recorded high to moderate quality, ranging from 2.5 to 5 percent coefficient of variation. Fabricator E recorded high to moderate quality except in the 6-mil diameter and 9-mil diameter vias, where the coefficient of variation was 12.7 percent and 92.9 percent, respectively. Fabricator F had moderate quality for 5-, 6-, 7-, 8-, 10-, 12-, and 13.5-mil diameter vias, but poor to very poor quality for remaining via sizes.

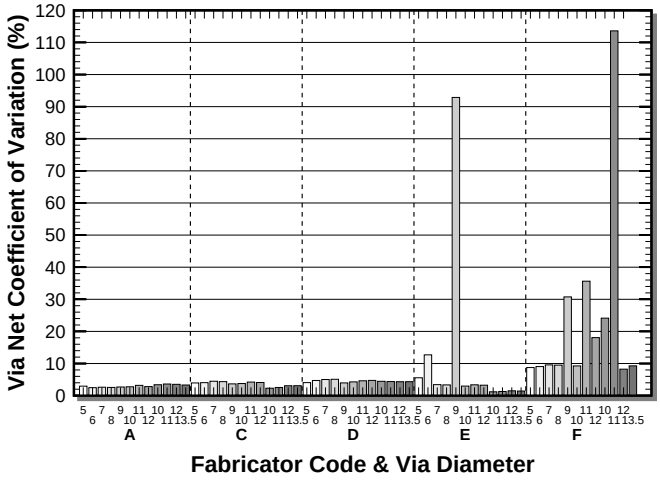

Figure 4. Via Quality Before Stress

Via defect densities are tabulated before and after environmental stress in Table 2, and Table 3, respectively. There were three panels from each of the fabricators A, C, D, and E, while there were 9 panels from Fabricator F. Thus, a single defect contributes to approximately 15 defects per million vias in the first four sets, and approximately 5 defects per million vias in the last set. The increased defect densities after stress reflect the additional failures caused by that

process.

Via Diameter (Mils)	Fabricator Code				
	A	C	D	E	F
5	0	0	0	627	0
6	0	0	0	75	10
7	0	0	15	60	5
8	0	0	0	0	0
9	0	0	0	72	19
10	0	0	0	0	9
11	0	0	0	0	5
12	0	0	0	0	19
10	0	28	0	0	1633
11	0	0	0	0	1274
12	0	0	0	0	648
13.5	0	0	0	0	230

Table 2. Via Defect Density Before Stress

Via Diameter (mils)	Fabricator Code				
	A	C	D	E	F
5	15	0	15	648	89
6	0	0	0	91	10
7	0	0	15	60	5
8	0	0	0	0	0
9	29	0	44	146	49
10	0	0	0	0	9
11	0	0	0	0	5
12	0	0	0	0	19
10	29	28	29	0	1776
11	0	0	0	0	1314
12	0	0	0	0	650
13.5	0	0	0	0	221

Table 3. Via Defect Density After Stress

The impact of environmental stress on via quality is illustrated for fabricator F in Figures 5, 6, and 7. The resistance after stress is plotted against the resistance before stress for each daisy chain measured. Figure 5 shows the results from the through vias, while Figures 6 and 7 show the results from one-deep and two-deep vias, respectively. Because there is such a wide range of resistances, the data are plotted on log scales. The solid diagonal line in each figure indicates no change in resistance due to stress, while the dashed line in each figure indicates 100 percent increase in resistance.

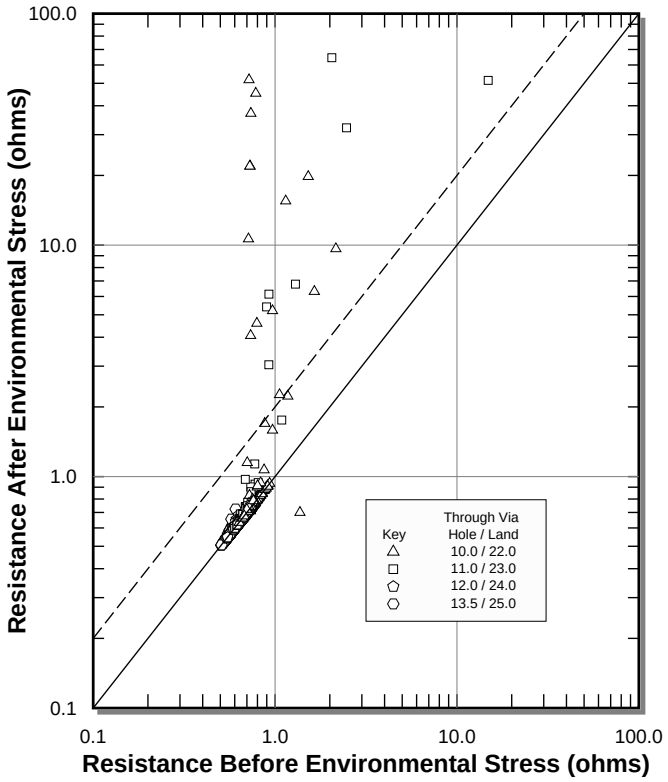

Figure 5. Through Via Stress Impact - Fabricator F

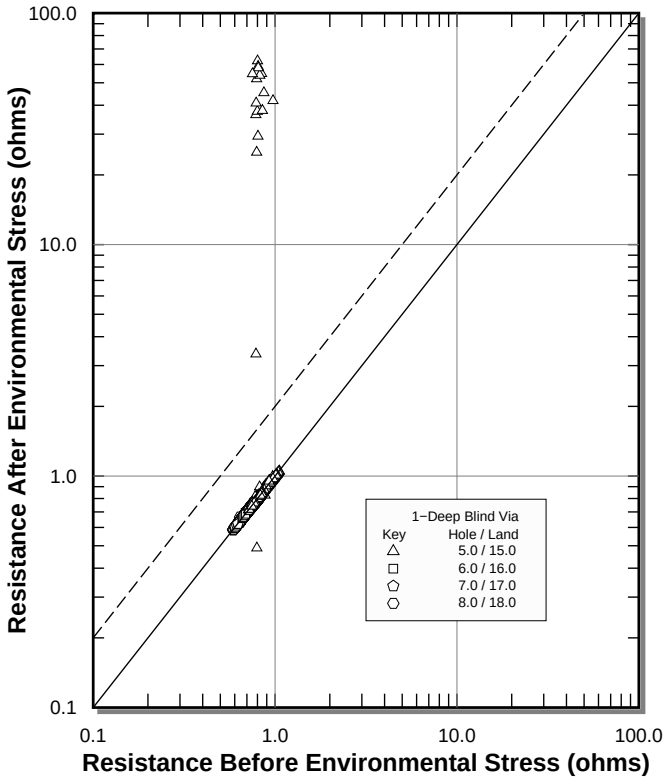

Figure 6. One-Deep Blind Via Stress Impact - Fabricator F

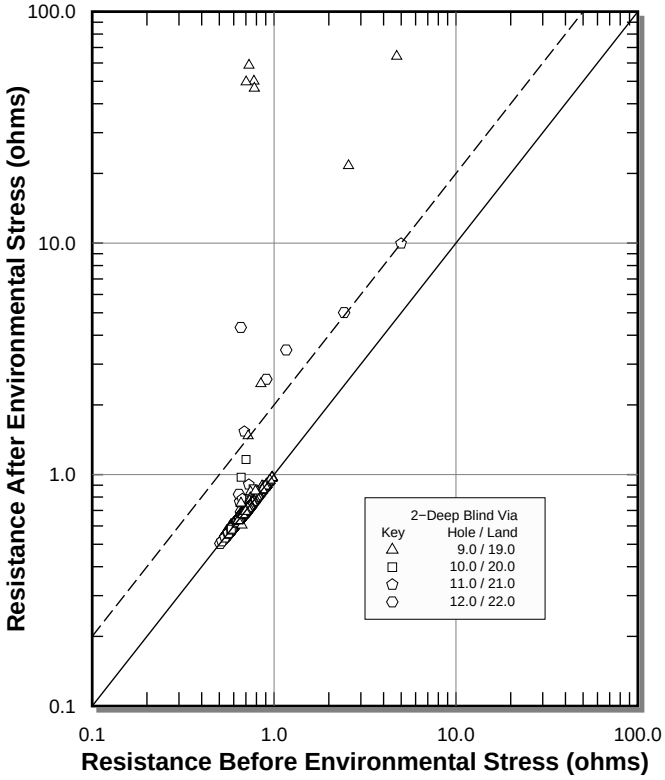

Figure 7. Two-Deep Blind Via Stress Impact-Fabricator F

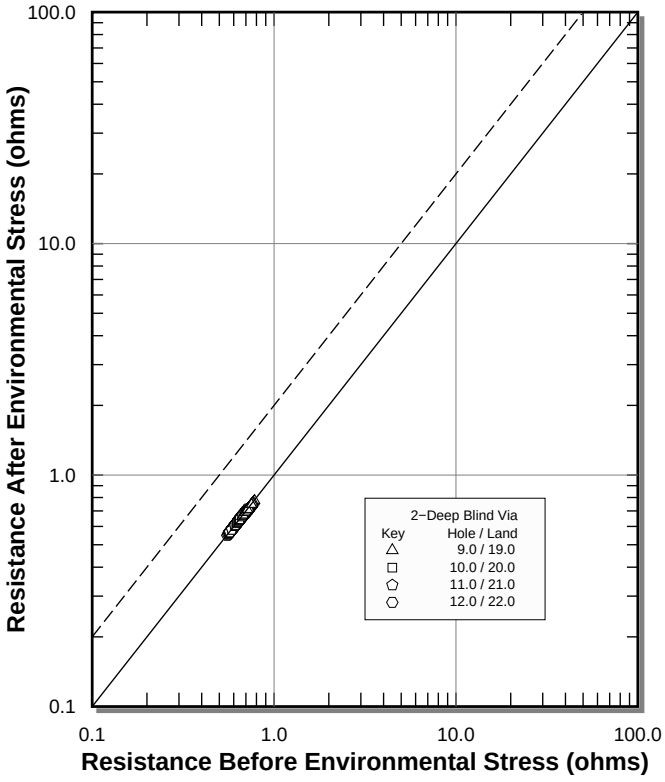

Figure 8. Two-Deep Blind Via Stress Impact-Fabricator C

In contrast to results from fabricator F, Figure 8 shows the impact of the stress on the two-deep vias manufactured by Fabricator C. Similar results were obtained for the one-deep vias and through vias manufactured by Fabricator C. Only one via net showed significant change after stress – a 10-mil diameter through via daisy chain increased in resistance from 0.658 ohms to 1.927 ohms.

Summary

As a part of a supplier management program, Teradyne Inc. asked their printed circuit board suppliers to fabricate process capability panels designed to assess manufacturing capability and product quality. In comparison to the first round, this second round of tests used relaxed design rules, because of the difficulty in forming, metallizing, and patterning blind vias.

The process capability panels were manufactured by each participating fabricator, and electrically tested to determine initial capability and quality. Subsequently, the panels were processed through a forced hot air convection oven to simulate an assembly operation, and re-tested to determine the effects of the stress. Via defect density (a measure of capability), via net resistance, and via net resistance coefficient of variation (a measure of quality) were the primary measures for comparison.

The results showed significant differences in capability and quality among the fabricators participating in the study. Poor capability and poor quality (observed before environmental stress) are indicators of reliability problems. However, good capability and quality as measured by defect density and resistance coefficient of variation, respectively, do not necessarily guarantee reliability. The diverse performances among the fabricators emphasize the difficult of metallizing high aspect ratio through vias and one- and two-deep blind vias.

Acknowledgments

CAT Inc. would like to thank David Evans of Teradyne Inc., Agoura Hills, CA, and Wayne King of Teradyne Inc., San Jose, CA, for their contributions to this column.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VI • Issue 6**

SIGNATURES FROM CONDUCTOR PROCESS CAPABILITY PANELS

A wealth of information is available from the fabrication, testing, analysis, and interpretation of data from conductor process capability panels. The data from these specialized test patterns identifies processing issues, and often points to possible solutions. This column begins a series of columns that examine signatures from test results that are characteristic of specific problems, and recommend a strategy to improve capability and quality.

Process Capability Panel

A schematic of the conductor process capability panel is illustrated in Figure 1. One-inch-square conductor modules cover the area of an 18 by 24-inch panel. The 16 rows and 22 columns of modules form a checkerboard pattern, with conductors in the shaded modules running vertically and the conductors in the non-shaded modules running horizontally. Each module has four conductors, which are separated by three spaces. This study had conductor widths of 2.0, 3.5, 5.0, and 6.5 mils, separated by spaces of 2.0, 3.5, and 5.0 mils, respectively.

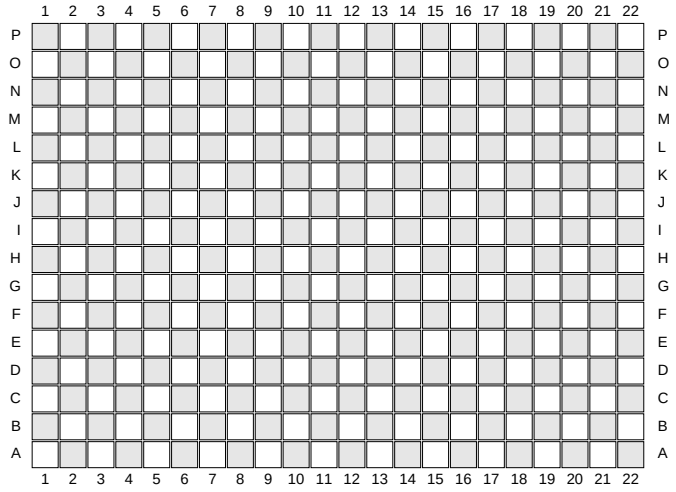

Figure 1. Conductor Panel Schematic

A set of ten panels was imaged, developed, etched and stripped under constant processing conditions in a benchmark study of a develop-etch-strip line. The results revealed a significant uniformity problem on the top side of the panels, which contributed to an abundance of defects in the smallest features. This non-uniformity is commonly observed in printed circuit board manufacturing,

The Signature

Conductor width uniformity over the surface of the panels facing up during developing and etching is illustrated in Figure 2. This three-dimensional rendering shows the conductor width for the nominal two-mil conductors averaged over the ten panels, and plotted as a function of position on the panel surface. The 16 rows and 22 columns, labeled A through P and 1 through 22, respectively, correspond to those shown in Figure 1, and indicate position on the surface of the panels. The plot clearly shows that the conductors are wider at the center of the panel than at the perimeter. The average conductor width was 1.03 ± 0.14 mils, with a minimum value of 0.71 mils and a maximum value of 1.43 mils.

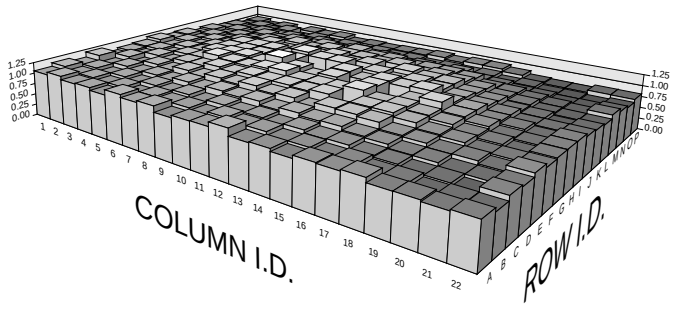

Figure 2. Conductor Width 3D Plot - 2-Mil Conductors

The placement of the four conductors within the module is fixed by the designed widths of the conductors and spaces. As finished conductors become narrower, the spaces delineating them become wider, and conversely, wider finished conductors lead to narrower spaces. With the variation in conductor width shown in Figure 2, it is not surprising that defects may occur, especially in the narrowest features.

Impact

In this particular benchmark, a strong correlation between conductor width and defects was observed. Figure 3 shows a map of "shorts" defects for the ten panels in the set as a function of nominal space width and position on the panel. Once again, the 16 rows and 22 columns, labeled A through P and 1 through 22, respectively, correspond to those shown in Figure 1. The map displays results from each module in three rectangles that represent the three space widths in the design, 2.0, 3.5, and 5.0 mils. Dots are placed in the rectangles for each panel having a "short" in the corresponding space and module. In a set of ten panels, zero dots (no defects) to ten dots (all panels defective) can be placed in each of the rectangles.

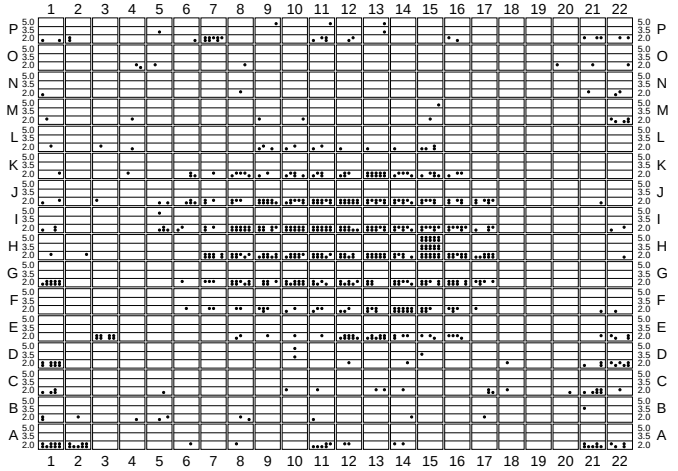

Figure 3. Defects Map - Shorts in Spaces

Referring to Figures 2 and 3, the concentration of "shorts" in the two-mil wide spaces corresponds to the wider conductors found toward the center of the panels. With the frequency of two-mil shorts observed in this process, there is a high probability of having many undetected "near-shorts" that can lead to reliability failures. Thus, the non-uniformity of the process limits practical designs to those with spaces that are much greater than two mils. Further, the conductor width variation resulting from this process also impacts electrical performance in terms of signal integrity and controlled impedance.

Contributing Factors

There are many possible sources of the non-uniformity measured in this benchmark. The three most-probable sources are 1) puddling in the developer, 2) puddling in the etcher, and 3) intensity variation in the printer. Other possible sources include variations in feature widths in the artwork, and off-contact between the artwork and the photoresist during the imaging step.

Recommendations for Improved Capability and Quality

This particular signature is a common problem found in printed circuit boards manufactured in horizontal developers and etchers. If illumination intensity is determined to be uniform, the artwork is acceptable, and the artwork is in "hard contact" during the printing step, one should consider running designed experiments on the developer and etcher. Adjustments to solution temperature, spray pressures, oscillation rates, volumetric flow rates, nozzle angles, and even nozzle design should be investigated.

Summary

Significant insight into the manufacturing process is available from the analysis of data collected from conductor process capability panels. Sources of defects and non-uniformity can be identified by fabricating specially designed patterns, testing the patterns, analyzing the data, and interpreting the results. A selection of conductor panel designs is available from CAT Inc., free of charge at '**http://biz.swcp.com/cat**'.

In this first column on *Signatures from Conductor Process Capability Panels*, wider conductor width at the center of the panels was correlated with an increased frequency of "shorts" in narrow spaces. This non-uniformity, frequently observed in innerlayer fabrication, is often caused by puddling in the developer or etcher, but could also be related to poor artwork, non-uniform intensity in the printer, and off-contact between the artwork and photoresist during printing.

The degraded uniformity impacts process yields, limits feature widths, and adversely affects the electrical performance of designs intended for high frequency applications. Once this signature is documented, process engineers can run designed experiments to identify sources of the problem, and implement process changes to improve capability and quality.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VI • Issue 7**

SIGNATURES FROM CONDUCTOR PROCESS CAPABILITY PANELS - II

In the last column, *Signatures from Conductor Process Capability Panels* related defects at the center of the top side of panels to process non-uniformity. The three most probable sources of the variation were puddling in the developer, puddling in the etcher, and intensity variation in the printer. Product manufactured by the process that was studied in the benchmark will exhibit characteristics similar to the test results – limiting feature widths, impacting yields, and affecting electrical performance.

This column examines results from another study, where the process transferred its signature to the bottom side of conductor process capability panels.

Process Capability Panel

The process capability panel that was used in this example is similar to the one in last month's column, with the exception of feature sizes. This design had 352 one-inch-square conductor modules arranged in 16 rows and 22 columns on an 18- by 24-inch panel. Each module had 3-, 4-, 5-, and 6-mil wide conductors, separated by 3-, 4-, and 5-mil wide spaces, respectively. Adjacent modules have conductors that are orthogonal to one another, forming a checkerboard pattern of horizontal and vertical lines.

The Signature

The width of the nominal three-mil wide conductors, averaged from the bottom side of the ten panels in this study, is displayed in the three-dimensional plot in Figure 1. The width of the finished conductors varied primarily by column, with conductors in columns 1-3, 12, and 20-22 wider than those in the other columns. The conductors averaged 2.73 ± 0.13 mils, with a minimum and maximum of 2.45 and 3.07 mils, respectively.

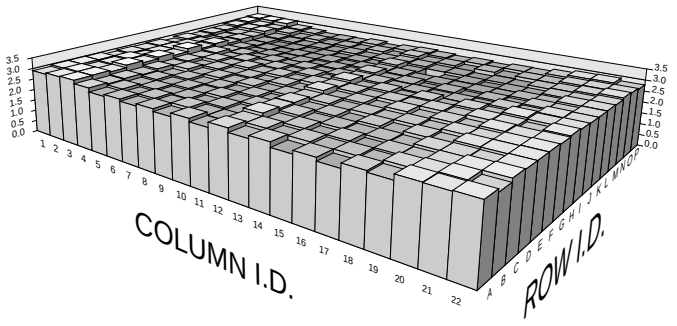

Figure 1. Conductor Width 3D Plot - 3-Mil Conductors

Impact

The conductor width non-uniformity displayed in Figure 1 is correlated with the frequency of "shorts" in the narrowest space in the pattern. Figure 2 displays feature yield averaged by column from the bottom side of the ten panels in this study. While the 3-, 4-, 5-, and 6-mil wide conductors, and 4- and 5-mil wide spaces recorded few defects, "shorts" in the 3-mil wide spaces were prevalent, especially in columns 1-3, 12, and 20-22.

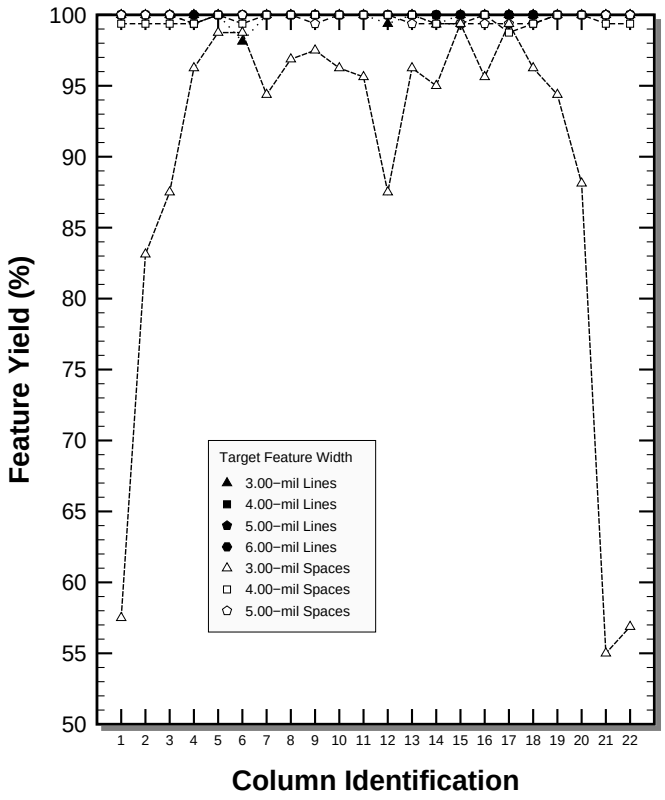

Figure 2. Conductor and Space Yield by Column

The effective space width may be calculated by adding the conductor width loss to the nominal space width. Thus, the effective space width increases as finished conductors become narrower. Space yield for the nominal 3-mil spaces, averaged by column over the ten panels, is plotted against effective space width in Figure 3. The trend line that is fit to the data highlights the dependence of space yield on space width. The data indicate that space widths below 3.5 mils are beyond the limit of the process studied here.

Contributing Factors

The signature on the panels as a result of the fabrication process is characteristic of conveyorized processing equipment. The panels were conveyed with row P as the leading edge in both the developer and etcher. Variations in finished conductor width, manifested by the stripes in the columns in Figure 1, are parallel to the direction of travel in the equipment. The most probable sources of the non-uniformity are 1) unbalanced spray pressures in the developer or etcher, 2) clogged nozzles in the developer or etcher, and 3) interference between the transport system and spray system that interrupts the delivery of developing or etching chemistry to the surface or the panel.

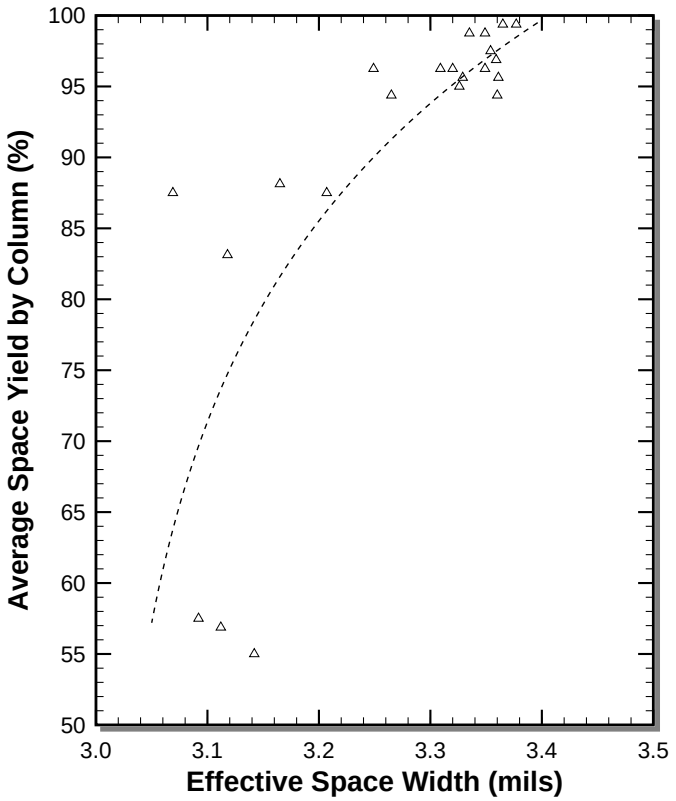

Figure 3. 3-Mil Space Yield vs. Effective Space Width

Recommendations for Improved Capability and Quality

Variations in conductor width that form stripes parallel to the process direction are usually related to spray delivery systems in either or both the developer and etcher. Well established inspection and maintenance procedures can help to eliminate intermittent episodes of the problem, while experiments that lead to equipment design changes or process changes may be required to eliminate consistent striping problems. As part of routine maintenance, inspect for (and clear) clogged nozzles, balance spray manifold pressures, ensure filtration systems (if present) are functioning, and keep the equipment clean.

Observe the location of the spray nozzles with respect to the conveyor transport system. If striping is caused by interrupted or blocked spray, the nozzles or conveyor may have to be modified. If the system is equipped with oscillating spray nozzles, changing the oscillation rate with respect to conveyor speed can impact uniformity.

Experiments to study uniformity can be designed to investigate the effects of conveyor systems, nozzle types, spray pressures, and oscillation rates. An initial benchmark documenting the non-uniformity, a designed experiment to study the effects of the variables, and a confirmation run to verify the changes can lead to improved manufacturing capability and product quality.

Summary

Poor conductor width uniformity lowers process yields, impacts capability, and degrades electrical performance. Stripes of varied conductor widths running parallel to the processing direction on conductor process capability panels are signatures characteristic of conveyorized processing equipment. Unbalanced spray pressures, clogged nozzles, and interference between the transport system and spray system in either or both the developer and etcher are possible sources of the problem.

While rigorous maintenance programs can minimize the intermittent occurrence of stripes due to clogged nozzles, designed experiments that study the effects of equipment design and processing variables may be necessary to eliminate non-uniformities inherent in the system. By processing conductor process capability panels (a selection of conductor process capability panel designs is available free of charge from CAT Inc. at '**http://biz.swcp.com/cat**') process engineers can collect the data to make sound decisions that will lead to improvements in manufacturing capability and product quality.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VI • Issue 8**

SIGNATURES FROM CONDUCTOR PROCESS CAPABILITY PANELS - III

In the previous two columns, puddling and striping were identified as signatures from conductor process capability panels. In both cases, defects were linked to conductor width variations, and both capability and quality were compromised.

This column continues the topic with the third signature, a checkerboard pattern related to the dependence of finished conductor width on conductor orientation.

Process Capability Panel

The process capability panel that was used in this study is shown schematically in Figure 1. One-inch-square conductor modules were arranged in 16 rows and 22 columns on the 18- by 24-inch panel. Each module contained four conductors, designed at 3, 4, 5, and 6 mils in width, which form a serpentine-shaped pattern over the module area. The four conductors were separated by spaces of 4, 5, and 6 mils, respectively. The modules were placed alternately with conductors running parallel and perpendicular to the 24-inch panel edge, forming the checkerboard pattern indicated in the figure. A selection of conductor process capability panel designs, similar to the one used in this study, is available free of charge from 'http://biz.swcp.com/cat'.

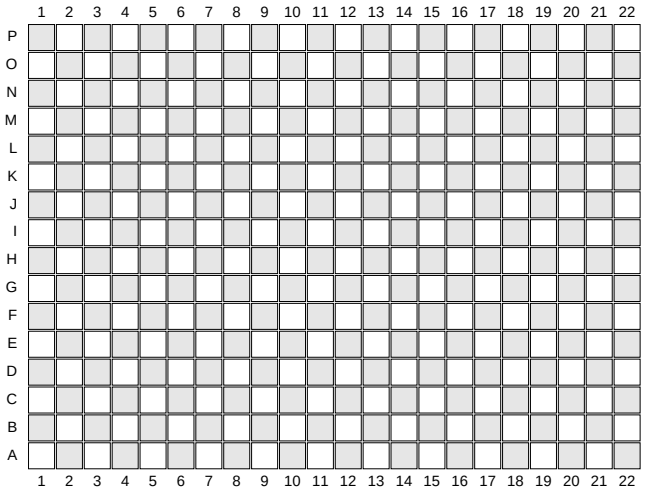

Figure 1. Conductor Panel Schematic

The Signature

The results from a benchmark of a develop/etch/strip line exhibited a strong dependence of finished conductor width on conductor orientation. Ten one-ounce copper-clad panels were imaged, developed, etched, and stripped under constant processing conditions. Figure 2 shows a three-dimensional rendering of conductor width, averaged by module over the top side of the ten panels in the set. The average width for the nominal 3-mil-wide conductor was 2.32 ± 0.18 mils with minimum and maximum of 2.02 and 2.81 mils, respectively. The width of conductors in horizontal modules, with conductors parallel to the 24-inch edge, is approximately 0.3 mils narrower than conductors in vertical modules. This bias is observed over the entire set of modules, and contributes substantially to the total variation.

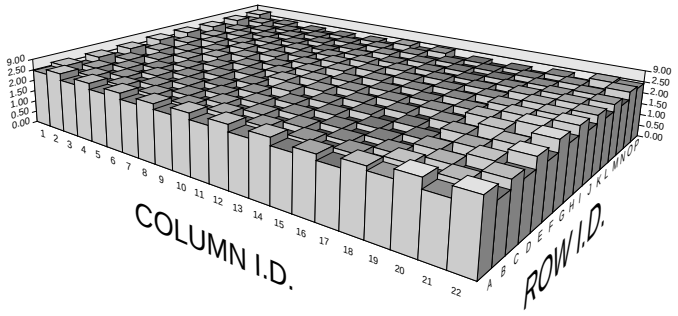

Figure 2. Conductor Width 3D Plot - 3-Mil Conductors

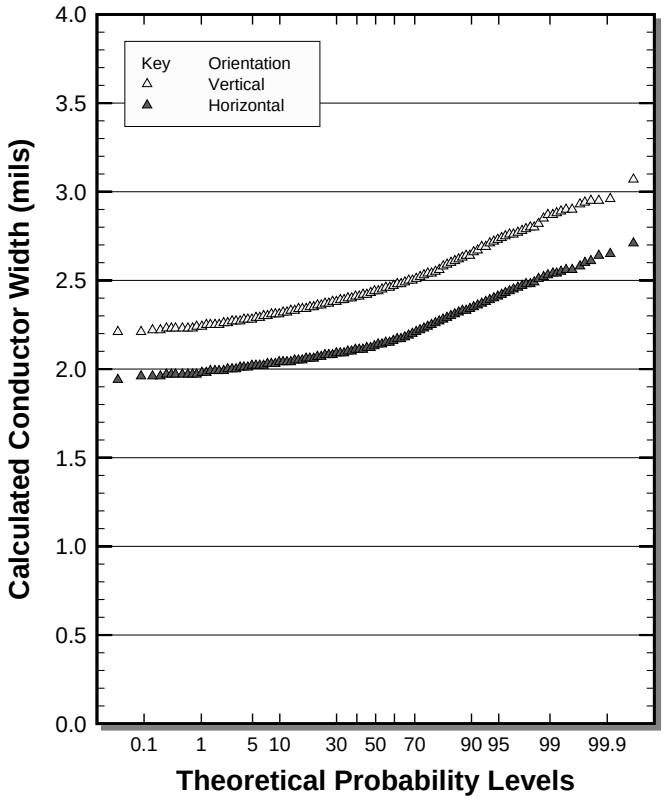

Figure 3. 3-Mil Conductor Width Distribution

Figure 3 displays the distribution of conductor widths from the top side of the ten panels. Calculated conductor width is plotted versus theoretical probability levels for vertically and horizontally orientated modules. The separation in the figure between vertical and horizontal conductors is 0.25 to 0.36 mils. If the data points form a straight line on this graph, the data are normally distributed with the standard deviation proportional to the slope. In both the vertical and horizontal sets, there is a break in the data at approximately 50 percent probability. This break indicates two populations, with the wider conductors in each set having larger standard deviations than the narrower ones. From Figure 2, it is evident that the widest conductors are located in columns 18-22 and row A.

Impact

The conductor width minimum, mean, maximum, range, standard deviation, and coefficient of variation are reported in Table 1 for the vertical modules, horizontal modules, and all modules combined. When examined separately, both the horizontal and vertical conductors exhibit moderate variation with a range from 0.77 to 0.86 mils, standard deviation from 0.124 to 0.134 mils, and coefficient of variation from 5.45 to 5.72 percent. The effect of the bias between vertical and horizontal conductors is seen in the combined results, with the range, standard deviation, and coefficient of variation increasing to 1.13 mils, 0.197 mils, and 8.52 percent, respectively.

Modules	Min (mils)	Mean (mils)	Max (mils)	Range (mils)	σ (mils)	CoV (%)
Vertical	2.21	2.46	3.07	0.86	0.134	5.45
Horizontal	1.94	2.16	2.71	0.77	0.124	5.72
Combined	1.94	2.31	3.07	1.13	0.197	8.52

Table 1. Conductor Width Statistics - 3-Mil Conductors

Although there was increased conductor width variation due to the horizontal/vertical bias, there was no correlation to an increase in "opens" or "shorts". The defects that were present appeared to be randomly distributed – independent of the horizontal/vertical bias and surface non-uniformity. Under the processing conditions that were used for this set of panels, the feature sizes were large enough to tolerate the spread measured in conductor width. However, if narrower features were to be manufactured by this process, one could expect the variations observed over the surface of the panels, compounded by the horizontal/vertical bias would lead to defects.

The increased variation in conductor width caused by this signature degrades electrical performance, especially in high frequency applications that require controlled impedance lines. The data show that a nominal 3-mil-wide conductor could measure from 1.94 mils to 3.07 mils in width, depending upon its placement and orientation on the panel. Since this data came from a set of panels that was processed under constant conditions, one after the other, additional variation should be expected from lot-to-lot, shift-to-shift, and day-to-day.

Contributing Factors

Possible sources of conductor width dependence on orientation include artwork and the fluid dynamics in the developer and/or etcher.

Most artwork generators that are used in printed circuit applications are laser raster scanning systems. The laser beam is modulated as it is scanned in a line in one direction over the surface of the film, while mechanical translation of the film relative to the beam provides coverage in the orthogonal direction. If the system is not set up properly, artwork features of a desired width running parallel to the scan direction can differ from those running perpendicular to the scan direction.

The developer and etcher provide chemical solutions to the surfaces of the printed circuit board as it is processed. If solution velocity differs in the horizontal direction compared to the vertical direction, then the chemical activity can become preferential in one direction compared to the other, accounting for a bias in finished conductor width.

Recommendations for Improved Capability and Quality

If the horizontal/vertical signature is observed from the manufacture, test, and analysis of conductor process capability panels, begin the investigation by measuring the artwork to determine if the widths are uniform in the horizontal and vertical directions. If a bias in the artwork is observed, notify the responsible engineers and work with them to resolve the problem.

If the artwork does not account for the conductor width bias observed in the process capability panels, plan and run a set of experiments designed to investigate the effects of spray nozzles, spray pressure, spray angle, oscillation rate, etc. in both the developer and etcher.

By determining the source of the horizontal/vertical signature (artwork, developer, etcher, etc.) and implementing process changes that eliminate it, improved conductor width uniformity will be realized.

Summary

The horizontal/vertical conductor width signature discussed in this column can remain unnoticed in product, but contributes to variation. By fabricating conductor process capability panels, testing the panels, and analyzing the data from the tests, the signature becomes apparent. Only after identifying the problem can progress be made toward understanding the source and eliminating the effect.

The horizontal/vertical bias increases conductor width standard deviation, degrades uniformity, and lowers quality. Electrical performance, especially in controlled impedance circuits designed for high frequency applications, may also be compromised.

Possible sources of the problem include artwork, the developer, and the etcher. Measurements of feature widths on the artwork can establish whether the artwork is a contributing factor. If artwork does not account for the disparity, designed experiments can be employed to study the developing and etching processes to determine their impact on the signature. The fundamental knowledge gained from these studies can eliminate the signature and lead to improvements in capability and quality.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VI • Issue 9**

SIGNATURES FROM CONDUCTOR PROCESS CAPABILITY PANELS - IV

As conductor and space widths become narrower, they are inherently more difficult to manufacture. Because of their decreased size, greater lengths of conductors and spaces fit within the manufacturing format, requiring decreased defect density to achieve the equivalent yield of larger features. Further, as conductors become narrower, tighter absolute control of conductor widths is essential to achieve the same relative variation of larger features. These factors emphasize the need to understand the sources of variation, so that improvements to manufacturing capability and product quality can be realized.

Often, the source of the variation imposed on the width of conductors can be traced to equipment limitations, set-up, or malfunctions. In the last three columns, signatures resulting from puddling, striping, and a conductor orientation bias were correlated with defects and shown to degrade uniformity. This column examines another signature observed in conductor process capability panels that adversely impacts manufacturing capability and product quality.

Process Capability Panel

The conductor process capability panel, illustrated in Figure 1, is similar to the ones used in the previous columns for this topic. One-inch-square conductor modules, illustrated in Figure 2, are arranged in 16 rows and 22 columns, and cover the surfaces of the 18- by 24-inch panels. Each module has four conductors designed at 4.5, 5.5, 6.5, and 7.5 mils in width, separated by three spaces of 3.5, 4.5, and 5.5 mils, respectively. The modules were placed alternately with conductors running parallel and perpendicular to the 24-inch panel edge, forming the checkerboard pattern indicated by the shading in Figure 1. A selection of conductor process capability panel designs is available free of charge from Conductor Analysis Technologies, Inc. at '**http://biz.swcp.com/cat**'.

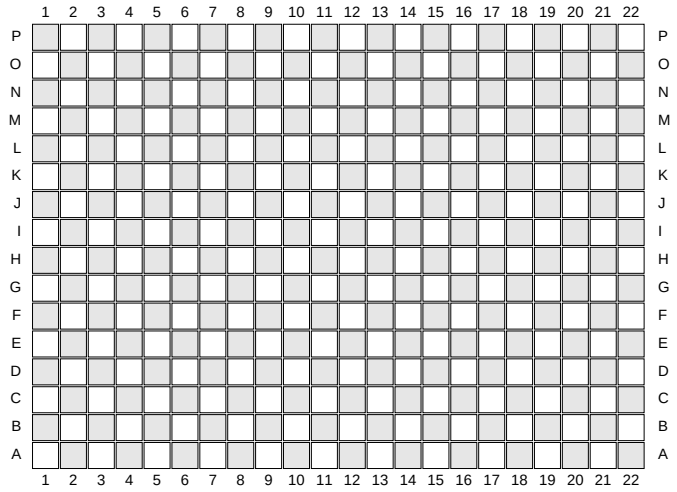

Figure 1. Schematic of a Conductor Process Capability Panel

Ten conductor process capability panels were manufactured as a benchmark of an innerlayer fabrication process. Dry film photoresist was laminated on both sides of substrates clad with one-ounce copper. The negative-acting photoresist was contact-printed on a non-collimated system, transferring the pattern to the resist. The panels were subsequently processed down a conveyorized develop-etch-strip line to complete the innerlayer fabrication process.

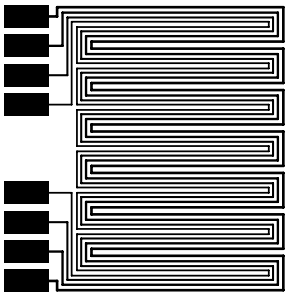

Figure 2. Schematic of a Conductor Module

The Signature

Figure 3 displays conductor width loss, averaged by module over the top side of ten panels, plotted versus module position on the panel. Conductor width loss is defined as the difference between the designed conductor width and the finished conductor width. As an example, if a conductor that is designed at 4.5 mils has a finished width of 3.25 mils, then the conductor width loss is 1.25 mils. The three-dimensional rendering shows considerable variation over the surface of the panels, with the greatest conductor width loss in columns 7-17, and the least conductor width loss in the two corners associated with rows A-E, and columns 1-4 and 19-22. In addition to the overall trend observed over the surface, there is a horizontal/vertical bias that is most pronounced in the areas with least conductor width loss.

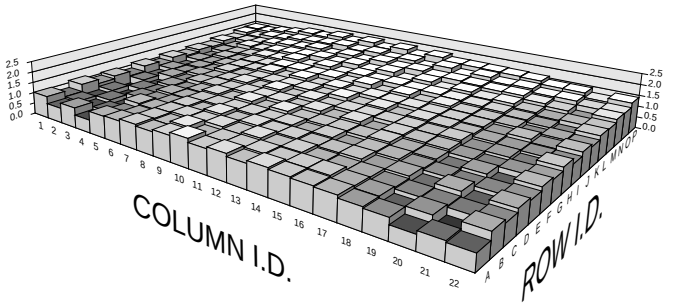

Figure 3. Conductor Width Loss 3D Plot

Impact

The impact of this signature is twofold – the increased conductor width variation leads to a reduction in quality, while the increased defect density due to shorts in the narrowest spaces leads to reduced capability. Table 1 shows the impact of the signature on conductor width uniformity. The minimum, mean, and maximum conductor width, along with the range, standard deviation, and coefficient of variation are reported for 4.5-mil (nominal) conductors for the entire population of 352 modules, and a reduced population of 224

modules.

Population	Min. Width (mils)	Mean Width (mils)	Max. Width (mils)	Range (mils)	σ (mils)	CoV (%)
352 Modules	2.45	3.36	4.71	2.26	0.277	8.25
224 Modules	2.45	3.27	4.14	1.69	0.242	7.40

Table 1. Conductor Width Uniformity Impact

With all modules from the ten panels included, the 4.5-mil (nominal) conductor varied from 2.45 to 4.71 mils in width, with a standard deviation of 0.277 mils and coefficient of variation of 8.25 percent. The results shown in Figure 3 indicate that the signature affects nearly all of the modules in columns 1-4 and 19-22. By excluding the 128 modules in these columns from the analysis, the remaining 224 modules show substantial uniformity improvement, reducing the range, standard deviation, and coefficient of variation to 1.69 mils, 0.242 mils, and 7.40 percent, respectively.

Figure 4 is a defects map, showing the location of "shorts" between the conductors from the ten panels in this set. Each module position on the panel surface is shown in the map as a square divided into three rectangles, one for each of the 3.5-, 4.5-, and 5.5-mil-wide spaces in the pattern. A dot is added to the rectangle if a "short" occurred in the corresponding space, module, and panel. Each rectangle can have from zero dots (no "shorts") to ten dots (every panel had a "short" in this space and module).

When comparing the defects in Figure 4 with the uniformity results in Figure 3, a strong correlation is apparent. The modules having the smallest conductor width loss (and therefore the widest conductors) have a concentration of "shorts" in the narrowest space.

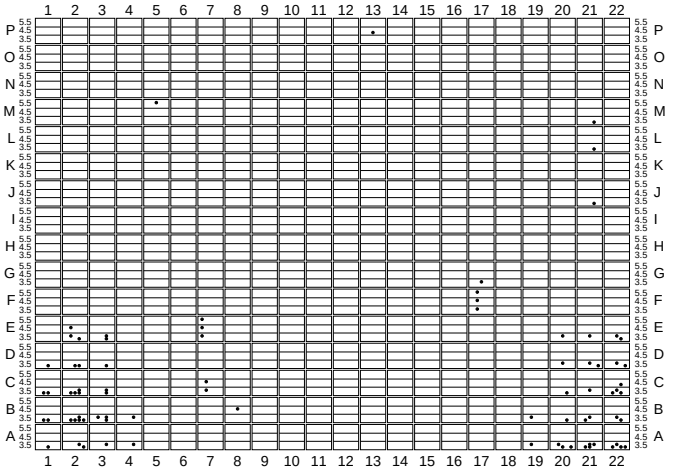

Figure 4. Defects Map - Shorts in Spaces

By identifying the source of the signature, investigating possible solutions, and making permanent process changes, considerable improvements can be realized in terms of manufacturing capability and product quality.

Contributing Factors

There are many possible causes of the non-uniformity shown in Figure 3. The completed pattern is the culmination of all the processing steps used in its manufacture, including artwork generation, imaging, developing, and etching. Un-balanced spray pressures in the developer and/or etcher, for example, are possible sources of the signature; but due to puddling, conductors are usually narrower at the panel edges than the middle. The artwork could account for the variation, but it is unlikely to have an impact this significant.

In this example, the source of the signature originated in the imaging process. The vacuum failed to hold the artwork in intimate contact with the photoresist over the entire panel area during the exposure step. Vacuum leaks or insufficient draw-down time prevented the artwork in columns 1-4 and 19-22 from contacting the photoresist. In areas of off-contact, the non-collimated ultra-violet source spread under opaque regions of the artwork, cross-linking wider features than intended in the resist, which ultimately define the conductors in the completed pattern.

Recommendations for Improved Capability and Quality

Begin by measuring the feature widths in the artwork to determine if the phototool can account for the variation observed in the data. Notify the artmaster staff of any uniformity issues measured in the photo tools, and work with them to resolve the problems.

In contact printing, look for the presence of Newton rings, which indicate that the artwork is in intimate contact with the photoresist. If off-contact areas are observed, check for an adequate vacuum level, adequate draw-down time, and check the seals for the presence of vacuum leaks. Correct the deficiencies, and confirm that the artwork is in hard contact with the photoresist.

For soft-contact or off-contact printing, check the uniformity, declination angle, and collimation angle of the illumination source. Make adjustments, if necessary, to bring these parameters into specification.

If the imaging system cannot account for the signature, check the spray pressures in the developer and etcher to determine if they account for the non-uniformity. It may be necessary to plan and run an experiment designed to evaluate the impact that spray pressure imparts on conductor width uniformity.

After making the processing changes, run another set of conductor process capability panels to confirm and document the improvements.

Summary

Variation from target conductor width reduces manufacturing capability and product quality. Often, signatures from the manufacture, testing, and analysis of conductor process capability panels can be traced to equipment limitations, equipment set-up, or equipment malfunctions.

In the example discussed in this column, conductor process capability panels that were contact-printed, developed, etched, and stripped had areas of wider-than-expected conductors along two edges of the panels. Off-contact between the artwork and the photoresist was identified as the source of the signature. A strong correlation between conductor width loss and "shorts" in the narrowest space in the pattern was apparent from the analysis. By ensuring adequate vacuum, adequate draw-down time, and by eliminating vacuum leaks in the printer, the variation from this signature can be eliminated. To confirm the improvements and document the results, another set of conductor process capability panels should be manufactured.

By identifying the source of the signature, investigating possible solutions, and making permanent process changes, considerable improvements can be realized in terms of manufacturing capability and product quality

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VI • Issue 10**

SIGNATURES FROM CONDUCTOR PROCESS CAPABILITY PANELS - V

The last four columns discussed signatures from conductor process capability panels that affect the width of conductors and spaces. The non-uniformities associated with the signatures were frequently correlated with defects, emphasizing the importance of understanding the source of the signature and eliminating it.

This column completes the series by examining a signature from a panel plating process that affects the uniformity of the conductor height.

Process Capability Panel

The conductor process capability panel, illustrated schematically in Figure 1, is 18 by 24 inches in size with 352 one-inch-square modules arranged in 16 rows (A-P) and 22 columns (1-22). The modules are placed horizontally and vertically over the area, forming the checkerboard pattern indicated by the shading in the figure.

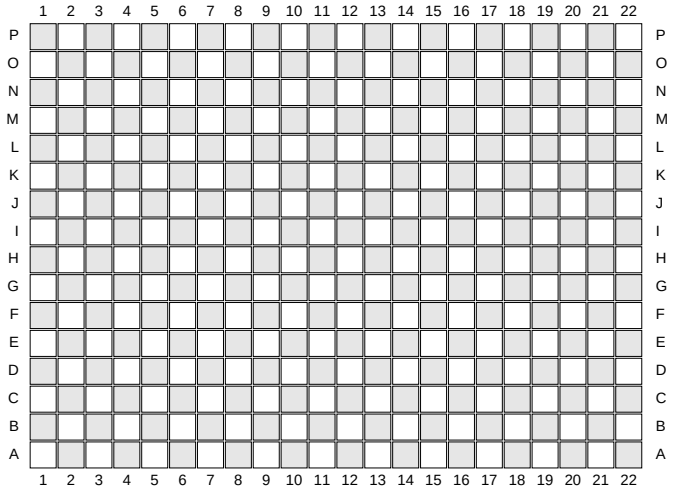

Figure 1. Conductor Process Capability Panel Schematic

Each module (Figure 2) contains four conductors separated by three spaces, which form a serpentine-shaped pattern over the module area. The conductors were 3, 4, 5, and 6 mils wide, and were separated by 3.5, 4.5, and 5.5 mil spaces, respectively. A selection of conductor process capability panels is available from CAT Inc., free of charge at '**http://biz.swcp.com/cat**'.

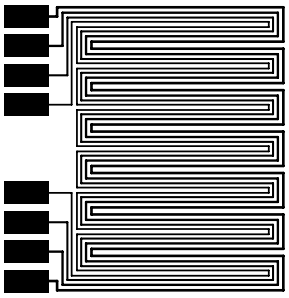

Figure 2. Conductor Module Schematic

The Signature

Figure 3 illustrates the plating thickness non-uniformity revealed in this set of panels. The data, averaged by module position, are collected from the bottom side of six process capability panels, fabricated in one lot under constant conditions. The three-dimensional rendering illustrates a common problem in electroplating processes – higher current densities at the perimeter of panels lead to increased plating rates compared to the middle of the panels. The minimum, mean, maximum, and standard deviation of copper thickness displayed in the figure are 1.58, 1.77, 2.21, and 0.11 mils, respectively. Because these statistics are based on average values over the six panels, the true range is much larger.

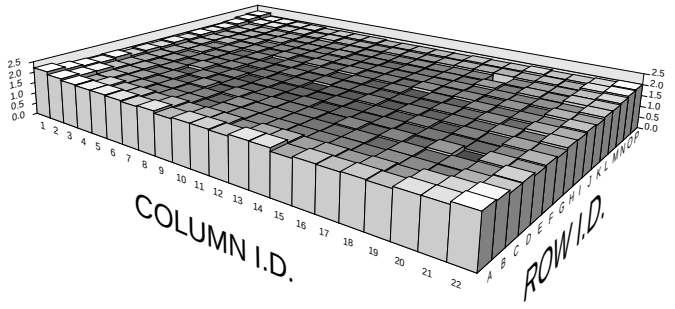

Figure 3. Conductor Height 3D Plot

Figure 4 displays a histogram of calculated conductor height collected from the modules on the bottom side of the six panels. These data illustrate the true range, with the minimum copper thickness measuring 1.39 mils, the maximum at 2.51 mils, and the mean copper thickness at 1.77 ± 0.15 mils. Clearly, significant plating variation occurred in the fabrication of the panels.

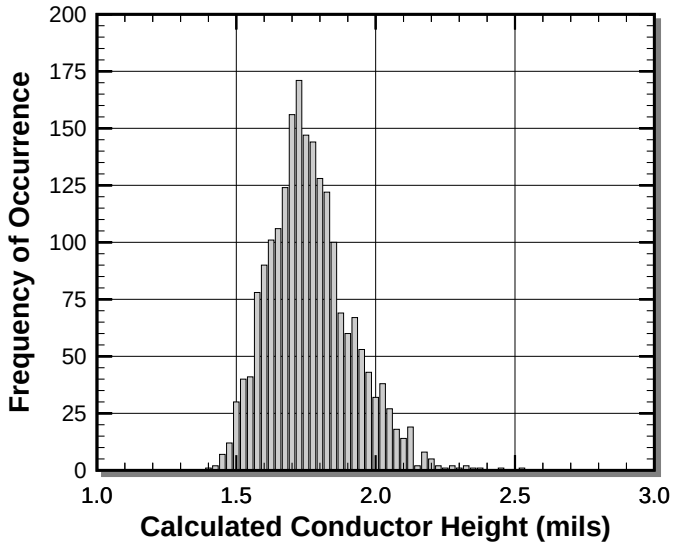

Figure 4. Conductor Height Distribution

To discover the sources of the total variation, the plating distribution for each of the six panels is displayed as box plots

in Figure 5. The results from each panel are similar, exhibiting a wide range and having outside values (indicated by the dots) on the upper end of the thickness scale. The variation over each panel is compounded by the shift in the median values (indicated by the notch) from panel-to-panel.

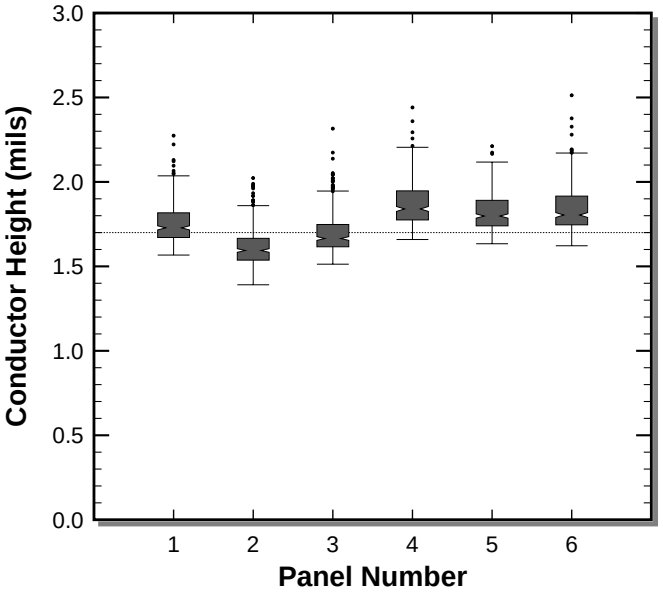

Figure 5. Conductor Height Distribution by Panel

The statistics, listed in Table 1, show that the maximum range for an individual panel is 0.89 mils, while the range for all panels combined is 1.12 mils. Thus, rack position in the plating cell impacts the average plating thickness and contributes to the overall variation.

Panel ID	Min Height (mils)	Mean Height (mils)	Max Height (mils)	Range (mils)	σ (mils)	CoV (%)
1	1.57	1.75	2.27	0.71	0.118	6.70
2	1.39	1.62	2.02	0.63	0.111	6.88
3	1.51	1.70	2.32	0.81	0.125	7.33
4	1.66	1.87	2.44	0.78	0.129	6.88
5	1.63	1.82	2.21	0.58	0.109	5.97
6	1.62	1.84	2.51	0.89	0.135	7.32
All	1.39	1.77	2.51	1.12	0.150	8.48

Table 1. Conductor Height Statistics by Panel

Additional insight into the signature is available by examining the copper thickness plotted by row (Figure 6) and by column (Figure 7). Both figures show the greatest conductor height at the edges of the panel. Figure 6 shows that the thickness uniformity, indicated by the size of the box and the extent of the bars, generally degrades across the panel, from row A to row P, while the results by column shown in Figure 7 are more consistent across the panel, with the largest variation in column 1.

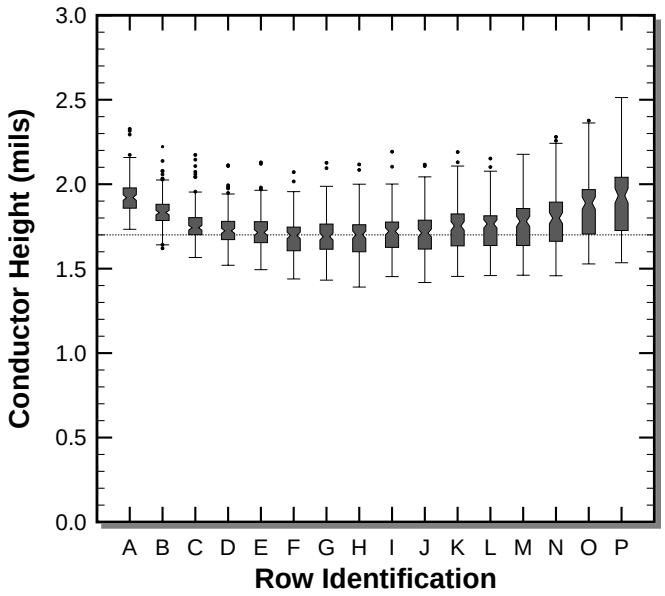

Figure 6. Conductor Height Distribution by Row

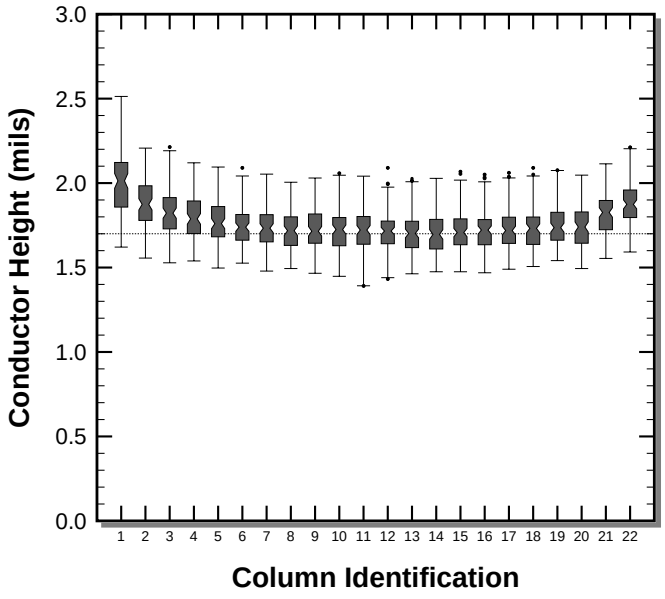

Figure 7. Conductor Height Distribution by Column

Impact

Copper thickness variation on printed circuit board surfaces can cause defects, limit conductor, space and via sizes, and lead to soldermask coverage issues and soldering faults during the assembly process. In pattern plating processes, for example, heavily plated areas may plate over the surface of the photoresist, making photoresist stripping incomplete and leading to "shorts". Narrow conductors and spaces formed by print-and-etch processes on thicker copper resulting from panel plated processes become difficult to form, reducing capability and quality. Thickness variations on conductors designed for controlled impedance will increase impedance

variation and degrade quality.

The plating thickness in vias usually depends on the copper thickness electroplated on the surface. Areas on the panel surface with the thinnest copper must be thick enough to achieve the minimum thickness requirements within the vias. Thus, copper thickness in vias in the higher current density areas can be much greater than desired.

Contributing Factors

Plated copper thickness depends directly on the current density at the cathode. Panel plating processes often have signatures similar to the example in this column, with increased plating thickness at the panel perimeter compared to the middle. Features formed by pattern plating often exhibit thickness variation that is dependent on the local conductor density; the current density at isolated conductors is greater than that of conductors in dense circuit areas. Rack position in the plating bath can impart additional variation from panel-to-panel.

Other factors affecting copper thickness uniformity include the plating chemistry, bath temperature, plating cell configuration, and solution agitation. Pulse plating may also have an impact on throwing power and thickness uniformity.

Recommendations for Improved Capability and Quality

An initial benchmark of the plating process will establish the extent of plating non-uniformity, and dictate whether improvements are necessary. This benchmark will show the uniformity over the surface of the panels, from side-to-side on panels, and from panel-to-panel, and serve as a yardstick against which process changes can be measured.

If the results of the benchmark indicate that plating uniformity needs improvement, plan and run a series of experiments designed to study effects of plating cell geometry, solution chemistry, agitation, current density, and direct current versus pulsed plating fields. Keep in mind that some of these parameters may affect the composition of the plated copper and physical properties, including tensile strength and ductility. If the experiments indicate that process changes will indeed improve thickness uniformity, run a confirmation benchmark. Also, measure the tensile strength and ductility of the copper plated under the new conditions to ensure that the reliability has not been compromised.

Summary

Non-uniform finished conductor height on printed circuit boards can adversely affect manufacturing capability and product quality. Minimum copper thickness requirements in vias, coupled with large variations in finished thickness over the surface of panels, from side-to-side on panels, and from panel-to-panel, can lead to vias in high current density areas with much greater copper than desired. Further, thickness non-uniformity can cause defects, limit conductor, space and via sizes, and lead to soldermask coverage issues and soldering faults during the assembly process.

The signature illustrated by the example in this column is commonly observed in panel plating processes, which often have higher current densities at the perimeter of panels compared to the middle. Pattern plating processes may have an additional signature superimposed on the one illustrated here, due to current densities that vary because of dense and sparse conductor areas on the printed circuit board surface. Side-to-side non-uniformity and variations from panel-to-panel also degrade overall product quality.

Control of conductor height can be quantified by the fabrication, testing, and analysis of data from conductor process capability panels. Results from designed experiments can be used to gain an understanding of plating non-uniformity, and provide the data to make process changes that will lead to improvements in manufacturing capability and product quality.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VI • Issue 11**

PHOTOPLOTTER IMPACT ON QUALITY

Laser photoplotters are commonly employed to create phototools that are used in the fabrication of printed circuit boards. Recent technological advances have led to systems with improved performance in terms of resolution and speed. As conductors and spaces decrease in width to achieve the demands of miniaturization, fabricators will find it necessary to replace photoplotters having one-quarter and one-eighth mil pixels with higher resolution systems having one-sixteenth or perhaps one-twentieth mil pixels.

Data provided by the designer describes the circuit board in an ideal sense. For example, conductors and spaces designed at specific widths will have a distribution of finished widths resulting from the superposition of the processing steps used in their manufacture. Imaging, developing, and etching each have an impact on the finished features. However, the conversion of design data to the finished circuit begins with laser systems that create the artwork. Imperfections, defects, and variation ingrained in the phototools at this step will be carried through to the finished product. This column examines the impact of photoplotters on finished conductor width.

Process Capability Panel

Figure 1 illustrates a schematic of the conductor process capability panel that was used in this study. The panel is 18 by 24 inches in size, with 352 one-inch-square modules arranged in 16 rows (A-P) and 22 columns (1-22). The modules are placed horizontally and vertically over the area, and form the checkerboard pattern indicated by the shading.

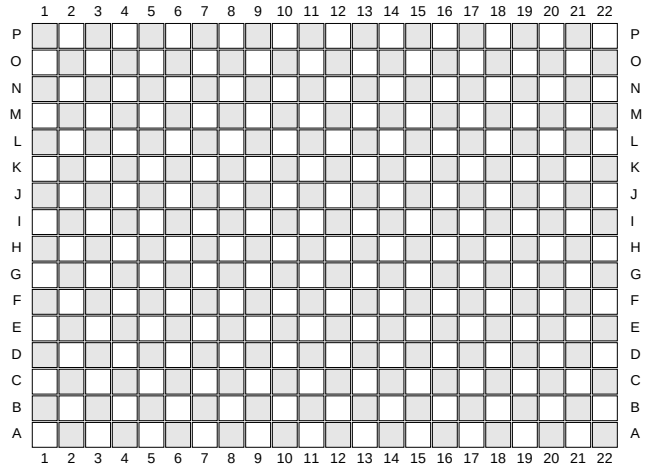

Figure 1. Conductor Process Capability Panel Schematic

Each module contains four conductors separated by three spaces, which form a serpentine-shaped pattern over the module area. The conductors were 3, 4, 5, and 6 mils wide, and separated by 4, 5, and 6 mil spaces, respectively. A selection of conductor process capability panels is available free of charge from CAT Inc. at '**http://biz.swcp.com/cat**'.

Procedure

A printed circuit board manufacturer ran experiments to investigate the impact of photoplotter resolution on finished conductor width. Silver halide polyester phototools for the experiment were plotted on two different photoplotters at different resolutions. Table 1 shows the plotter code and corresponding resolution for each of the four sets.

Set Number	Photoplotter Code	Pixel Size (mils)	Resolution (DPI)
1	A	0.050	20,000
2	A	0.125	8,000
3	B	0.125	8,000
4	B	0.250	4,000

Table 1. Photoplotter Resolution

Forty 18 by 24 inch panels clad with one-ounce copper on both sides were selected from the same raw material lot, pre-cleaned, and photoresist was applied. Following photoresist application, the panels were imaged sequentially on the same printer from set 1 through set 4, with a short delay between sets to change the phototools. Next, the panels were processed consecutively in a develop-etch-strip line, within 30 minutes time of completing the last image.

Five panels from each set were electrically tested, and the data was analyzed to establish the impact of photoplotter resolution on conductor width uniformity.

Results

Figure 2 displays conductor width standard deviation plotted versus photoplotter resolution, reported in dots per inch. The data are partitioned by panel side. Results from the top side show an increasing trend with increased resolution, while the results from the bottom side show a decreasing trend. Finished conductor width is influenced by many process steps, including imaging, developing, and etching. The developing and etching steps had a greater impact on the top side of the panels than the bottom side, primarily because of puddling in those processes. Because the relative impact of the imaging process is greater on the bottom side of the panels, only these data are investigated further.

Table 2 summarizes conductor width uniformity for 3-mil (nominal) conductors from the bottom side of the panels. The statistics are based on more than 1,740 conductors from each set of panels. The target conductor width was 2.0 mils for the nominal 3-mil design.

Figure 3 shows conductor width distribution, plotted by panel for the 3-, 4-, 5-, and 6-mil-wide conductors on the bottom side of the panels. The data are displayed as notched box plots, with the median centered at the notch. The box encompasses the interquartile range and extends from the 25th to the 75th percentile, while the adjacent values (bars) generally show the range. If data are greater than the upper quartile plus 1.5 times the interquartile range or less than the lower quartile minus 1.5 times the interquartile range, then they are plotted as dots and designated as outside values.

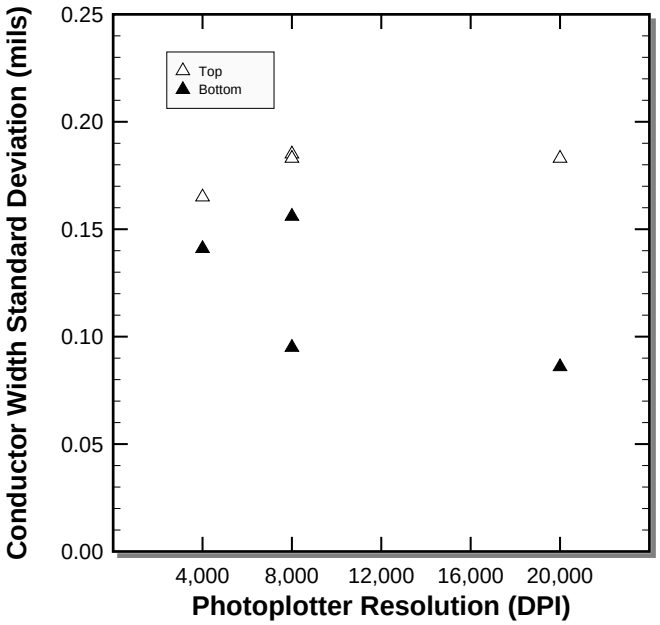

Figure 2. Conductor Width Standard Deviation vs. Photoplotter Resolution

Photoplotter Code	Resolution (DPI)	Mean (mils)	Range (mils)	Std. Dev. (mils)
A	20,000	1.76	0.49	0.086
A	8,000	1.61	0.66	0.095
B	8,000	1.69	1.03	0.156
B	4,000	1.89	1.06	0.141

Table 2. Conductor Width Results - 3-mil Artwork

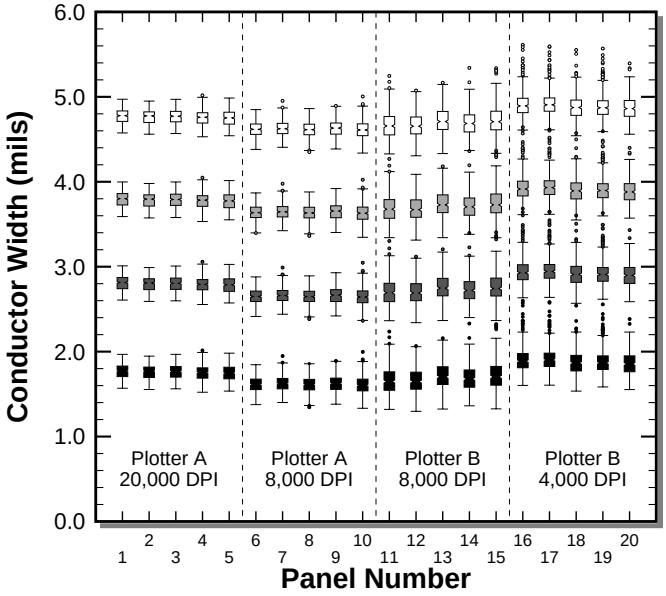

Figure 3. Conductor Width Distribution by Panel – Bottom side

Fabricated with artwork that was plotted at 20,000 dots per inch on photoplotter A, panels 1-5 exhibited the tightest control on conductor width, while panels from the other sets had broader distributions and an increased frequency of outside values. With the exception of panel number 8, the outside values erred on the side of wider conductors so the dots that extend into larger conductor width distributions belong to their narrower neighbors.

Results from the sets plotted at 8,000 dots per inch on two different photoplotters exhibit significant differences in uniformity. The standard deviation of 3-mil-wide (nominal) conductors in panels 6-10 from plotter A was 0.095 mils, while that of panels 11-15 from plotter B was 0.156 mils. The source of the disparity is revealed by examining the uniformity over the surface of the panels.

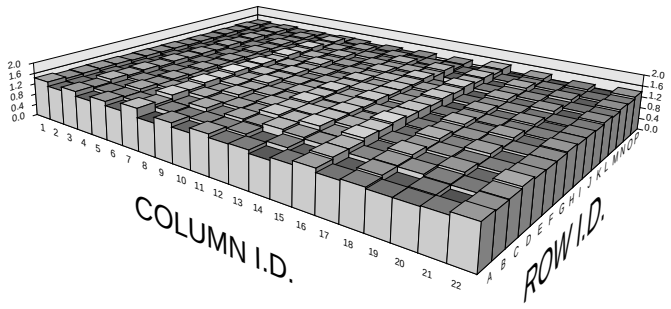

Figure 4. Conductor Width Loss - Bottom Side Plotter A – 8,000 DPI

Figure 4 displays a three-dimensional rendering of conductor width loss, averaged by module position over the bottom side of the five panels fabricated with photoplotter A at 8,000 dots per inch. Conductor width loss is defined as the difference between the designed conductor width and the finished conductor width. The mean conductor width loss for the data displayed in the figure was 1.37 ± 0.091 mils, with a minimum and maximum of 1.11 and 1.62 mils, respectively. The figure shows the effects of unbalanced spray pressures, blocked nozzles, or interrupted spray streams in the developer and/or etcher, which resulted in the stripes running from row A to row P, parallel to the direction of travel through the equipment.

In contrast, results from the five panels manufactured with photoplotter B at 8,000 dots per inch are shown in Figure 5. The three-dimensional plot shows a strong horizontal/vertical bias, with vertically positioned modules (conductors running parallel to the 18-inch panel edge) having greater line width loss than horizontal ones. These data have a mean conductor width loss of 1.29 ± 0.148 mils, with a minimum and maximum of 0.80 and 1.65 mils, respectively. While some evidence of stripes is shown in the figure, the prevailing signature of non-uniformity is the horizontal/vertical bias.

Summary

Laser photoplotters are commonly used to create phototools from design data, by patterning opaque and clear regions in polyester or glass, coating with silver halide or other

photosensitive materials. This first-removed copy of the design data will have imperfections, flaws, and variation depending on the limitations of the photoplotter systems employed. Proper setup and calibration are essential to minimize plotting errors.

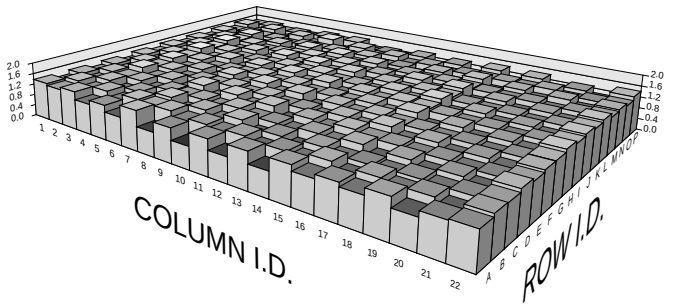

Figure 5. Conductor Width Loss - Bottom Side Plotter B – 8,000 DPI

A printed circuit board manufacturer studied the impact of photoplotter resolution on finished conductor width. Two photoplotters were investigated: plotter A at 8,000 and 20,000 dots per inch, and plotter B at 4,000 and 8,000 dots per inch. Plotter A, which is capable of higher resolution, provided more uniform conductor widths than plotter B.

Significant differences were observed between the systems upon comparing their performance at the same resolution (8,000 dots per inch). Plotter A recorded a standard deviation for 3-mil wide (nominal) conductors of 0.095 mils, while plotter B recorded a standard deviation of 0.156 mils for the same conductors. Further analysis revealed that a strong horizontal/vertical bias, present in the panels from plotter B, was the source of the disparity. It is not known whether calibration of the slow and fast scan directions for plotter B would eliminate the problem, or if the bias is a fundamental limitation of this particular system. However, the data clearly shows that photoplotters can be the source of the horizontal/vertical bias.

As conductor and space widths become narrower, higher resolution photoplotters will be required to provide the precision and accuracy necessary to manufacture quality products. Existing systems with resolutions of 4,000 and 8,000 dots per inch will be replaced with higher-resolution systems capable of 16,000 to 20,000 dots per inch. Prior to the commitment of capital expenditures necessary to purchase and install a new photoplotter, it is prudent for fabricators to benchmark available systems to ensure the system they select will satisfy their requirements for capability and quality.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VII • Issue 4**

IPC D-36 PCQR^2 SUBCOMMITTEE

The IPC D-36 subcommittee titled "***Printed Board Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard***" was formed in order to develop an industry standard for process capability test panel designs, and to establish a database of test results from printed circuit board fabricators. The subcommittee membership is comprised primarily of Original Equipment Manufacturers (OEMs), Contract Electronics Manufacturers (CEMs), and Printed Circuit Board (PCB) fabricators.

Background

Tim Estes of Conductor Analysis Technologies, Inc., presented a paper titled *HDIS Capability Overview* at the IPC Spring Expo2000 Presidents Meeting. Many attendees were familiar with CAT technology, having fabricated CAT process capability panels as part of supplier management procedures, and for internal benchmarking and process improvement programs. At the conclusion of the presentation, Bill Beckenbaugh of Sanmina Corporation and Greg Lucas of Tyco Printed Circuit Group requested that the IPC develop a standard for the design of CAT process capability panels. The discussion emphasized that a standard would reduce the numbers of process capability panel designs that the fabricators would have to manufacture, while satisfying the need of the OEM/CEM community.

The outcome of the discussions from the Spring Presidents Meeting was a subsequent meeting held September 11, 2000 at the IPCWorks in Miami, Florida. Based on this meeting, the Technical Activities Executive Committee approved the formation of the D-36 subcommittee, and Thomas D. Newton of Manufacturers' Services Ltd., and David L. Wolf of Sanmina Corporation were selected as subcommittee Chairman and Vice-Chairman, respectively.

Subcommittee Charter

The IPC D-36 Subcommittee's charter is to establish and maintain a family of benchmark process capability panel designs, develop and maintain an anonymous database of printed circuit board suppliers' capabilities, and develop a companion standard within the IPC-2XXX family of design documents.

Design Library

The PCQR^2 Design Library includes 6-, 12-, 18-, and 24-layer designs, each with medium and high technology design rules. The designs incorporate conductor and space, via registration, through-, blind-, and buried-via hole formation, soldermask registration, and single-ended and differential impedance modules. The design feature sizes have been established, with overlaps between the medium and high technology counterparts. The PCQR^2 Design Library can be accessed at http://biz.swcp.com/cat.

Database

Data from the test panels will be compiled into an anonymous database that details the process capability, quality, and relative reliability demonstrated by PCB suppliers. The cost of developing and maintaining the database will be shared among PCB suppliers, OEMs, and CEMs. Suppliers will produce the process capability panels, pay for a portion of the testing and analysis services, and receive a report detailing the capability and quality of the panels submitted. Suppliers will have access to the database for six months following the posting of their data, which will allow them to compare their capability and quality to others.

OEMs and CEMs may use the database to find, screen, and select PCB suppliers based on technology requirements. They will have access to the database through an annual subscription. Although the database is anonymous, OEMs and CEMs can request the identity of the suppliers in the database. Requests will be forwarded to the appropriate supplier, who may contact the OEM/CEM directly. Examples of the PCQR^2 Database can be accessed at http://biz.swcp.com/cat.

Benefits

The PCQR^2 Database will offer benefits to PCB suppliers, OEMs, CEMs, and the IPC. Suppliers will collect quantitative data on process capability and quality, obtain direction for process improvements, technology developments, and road maps, and obtain a direct comparison to other fabricators. Because there are a limited number of PCQR^2 designs, suppliers will have fewer designs to manufacture as part of their customers' supplier management procedure. OEMs and CEMs can determine their supply base capability and quality, establish and maintain design guidelines, tailor designs for manufacturability, and obtain quantitative data for road maps. Similarly, the IPC will acquire quantitative data for industry road maps and design guidelines, and directions for industry R&D efforts.

Summary

Established by the IPC, the PCQR^2 subcommittee has the potential to streamline the PCB procurement process. To date, the subcommittee has developed a library of process capability panel designs. The information collected from the manufacture, test, and analysis of the PCQR^2 designs will provide quantitative data on manufacturing capability, quality, and relative reliability. The information will be compiled into the PCQR^2 Database to provide a convenient means to compare and contrast the capability, quality, and relative reliability of participating suppliers. The PCQR^2 standard will offer benefits to PCB suppliers, OEMs, CEMs, and the IPC.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VII • Issue 10**

IMPACT OF COPPER THICKNESS ON QUALITY – PART 1

The materials, equipment, and processes used in the fabrication of printed circuits determine the quality of the boards manufactured, and impact the performance and reliability of the finished product. Given an acceptable selection of materials and viable processing equipment, subtle processing variations can lead to defects or reduce the accuracy and precision of the finished features. This column examines the impact of copper thickness on finished conductor width and controlled impedance. Next month's column will continue the discussion, exploring the impact of copper thickness on via quality and reliability.

Process Capability Panel

The data for this column is from the IPC-010A design, an 18- by 24- by 0.062-inch, 12-layer process capability panel with: conductor/space modules on outerlayers, half- and one-ounce innerlayers, and buried core layers; through vias, one- and two-deep blind vias, and buried vias; and five unique impedance module designs. Thirty panels, fabricated in three lots of ten panels each, were submitted by a fabricator for testing and analysis.

Copper Thickness

Figure 1 displays outerlayer conductor height (equivalent to copper thickness) versus panel number for 20 of the 30 process capability panels. Conductor width and height are calculated from the precision electrical resistance measurements taken from the four nets within each conductor module. The data are displayed as notched box plots, with the notch centered at the median and the box extending from the 25th to 75th percentile, while the bars show the range of the data. The open circles in the figure are drawn at the mean conductor height values, and the dashed lines are drawn at ± 0.4 mils about the mean.

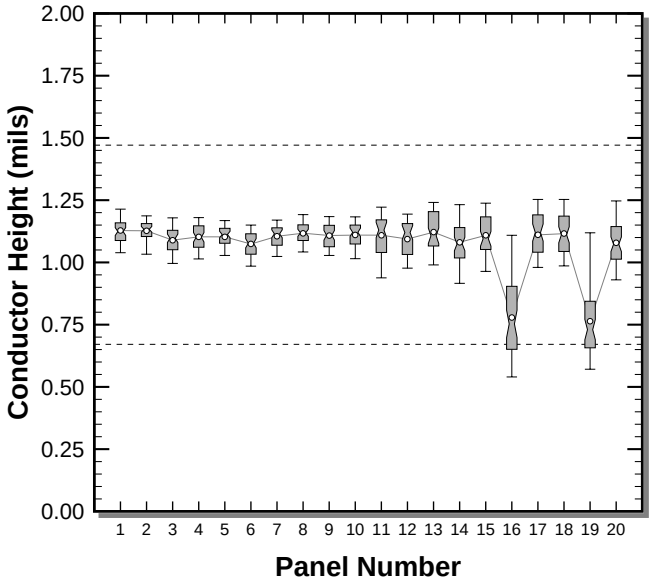

Figure 1. Outerlayer Conductor Height by Panel

The conductor height results from panels 1-10, fabricated in the first lot, exhibit greater precision than conductor height from panels 11-20, fabricated in the second lot. Average copper thickness for panels 1-10 was 1.11 mils with a standard deviation of 0.05 mils, while the average for panels 11-15, 17,18, and 20 was 1.10 mils with a standard deviation of 0.08 mils. Panels numbered 16 and 19 had thinner copper than the other eight panels in lot 2, with an average thickness of 0.77 mils and standard deviation of 0.34 mils. Possible sources of the disparity include inadequate plating time, lower current density, changes in plating chemistry, and poor electrical contact to the panels during plating.

Impact of Copper Thickness

Figure 2 shows conductor width for the nominal five-mil line on the outerlayers plotted versus panel number. Once again, a significant difference is observed between the two lots. Lot 2 has many outside values, indicated by the dots that extend beyond the bars.

The mean conductor width for the ten panels in lot 1 was 4.35 mils with a standard deviation of 0.28 mils. The mean conductor width for eight panels in lot 2 (excluding panels 16 and 19) was 4.30 mils with a standard deviation of 0.47 mils. Conductors on panels 16 and 19 were much narrower, with a mean width of 3.88 mils and a standard deviation of 0.44 mils. If the fabrication process employed panel plating, print-and-etch to form the features, the etchant would break through the thinner copper sooner than the thicker copper, accounting for narrower conductors.

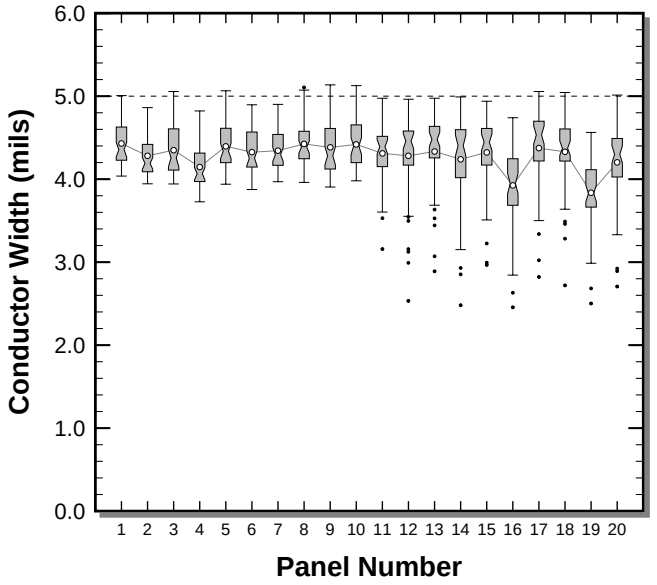

Figure 2. Outerlayer Five-mil Conductor Width by Panel

The impedance of a trace on an outerlayer (surface microstrip configuration) depends primarily upon the dielectric constant, dielectric thickness between the trace and ground plane, the trace width, and to a lesser degree conductor height. For a given dielectric constant and dielectric thickness, impedance increases with decreased trace width, but decreases with decreased trace height.

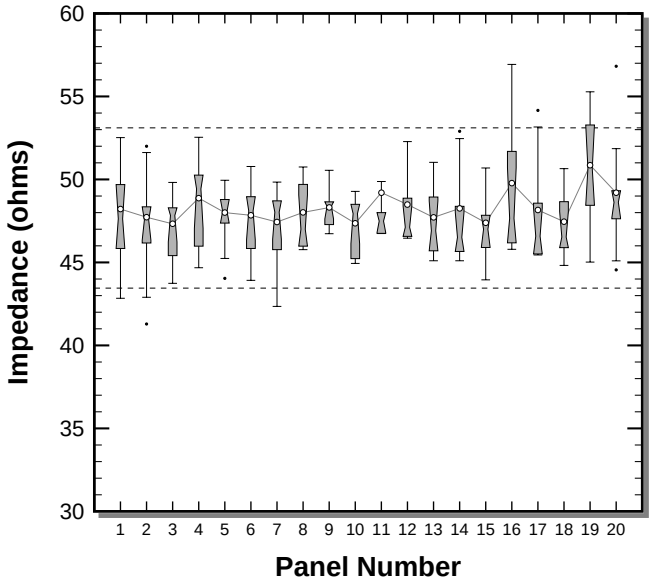

Figure 3. Surface Microstrip Impedance by Panel

The consequence of decreased trace width, moderated by decreased trace thickness is shown in Figure 3 for panels 16 and 19, compared to the other panels. The dashed lines in the figure are drawn at ± 10 percent about the average impedance for the 20 panels. The average impedance for panels 1-10 that were fabricated in lot 1 was 47.9 ohms with a standard deviation of 2.24 ohms. The average impedance for panels fabricated in lot 2 (excluding panels numbered 16 and 19) was 48.2 ohms with standard deviation of 2.86 ohms, while the average impedance for panels 16 and 19 was 50.3 ohms with standard deviation of 3.47 ohms. Thus, the decrease in copper thickness on panels 16 and 19 compared to the other panels in the two lots caused decreased outerlayer conductor widths, and in turn increased impedance in surface microstrip controlled impedance traces.

Summary

The quality of printed circuit boards depends upon the materials, equipment, and processes used in their manufacture. With continuing trends toward increased bandwidth, functionality, and smaller packages, tighter control on feature dimensions is necessary to achieve the signal integrity required by many applications. Even when the latest materials and manufacturing equipment are available, processes must be tightly controlled to provide consistent results at every step.

The variations in outerlayer copper thickness discussed in this column lead to narrower conductors, and increased impedance in surface microstrip structures. Without improvements in outerlayer copper thickness uniformity, signal integrity on product that is designed with surface microstrip controlled impedance structures will be questionable.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VII • Issue 11**

IMPACT OF COPPER THICKNESS ON QUALITY – PART 2

Discussions in the last column illustrated the effect that copper thickness can have on conductor width and controlled impedance. When etching different copper weights under identical processing conditions, thin copper will usually produce narrower conductors than thick copper, and the resulting change in conductor width affects the impedance of the net. This column continues the discussion by examining the impact of copper thickness on via quality and reliability.

Process Capability Panel

The data for this column was obtained from the same panels discussed in the last column. The design was the IPC-010A from the ***Printed Board Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard and Database*** design library. This is a high-technology, 18- by 24- by 0.062-inch, 12-layer process capability panel with: conductor/space modules on outerlayers, half- and one-ounce innerlayers, and buried core layers; through vias, 1- and 2-deep blind vias, and buried vias; and five unique impedance module designs. Thirty panels, fabricated in three lots of ten, were submitted by a fabricator for testing and analysis.

Copper Thickness

Figure 1 displays outerlayer conductor height (equivalent to copper thickness) versus panel number for 20 of the 30 process capability panels. Conductor width and height are calculated from the precision electrical resistance measurements taken from the four nets within each conductor module. The data are displayed as notched box plots, with the notch centered at the median and the box extending from the 25th to 75th percentile, while the bars show the range of the data. The open circles in the figure are drawn at the mean conductor height values, and the dashed lines are drawn at ± 0.4 mils about the mean.

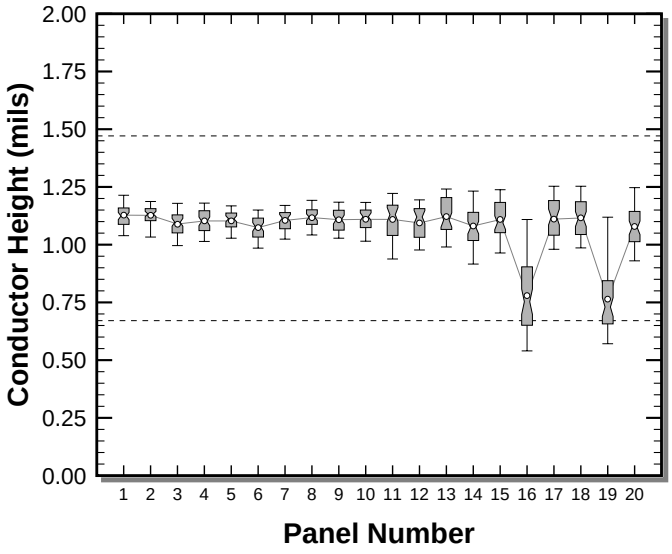

Figure 1. Outerlayer Conductor Height by Panel

Recall from last month's column that the copper thickness was more precisely controlled in the first lot of ten panels than the second lot. Additionally, panels numbered 16 and 19 had significantly thinner copper on the surface than the other eight panels in the second lot.

Plating thickness in through vias will generally track plated copper thickness on the surface of the panel. If this premise holds in this case, panels numbered 16 and 19 will have thinner copper in the vias.

Impact of Copper Thickness

The through-via modules in the process capability panel had 8-, 10-, 12-, and 13.5-mil diameter holes, each with 5-mil annular rings. Each daisy chain consisted of 92 through vias with an interconnect sequence of layers 1-7-2-8-3-9-4-10-5-11-6-12. Figure 2 shows the daisy chain resistance distributions for each hole size, plotted as notched box plots. The outside values, indicated by the dots in the figure, extend significantly beyond the majority of the data for each hole size.

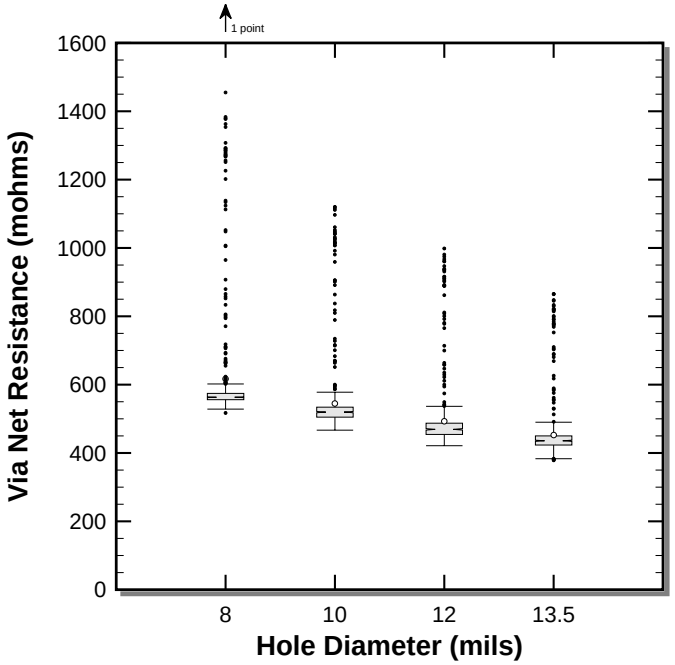

Figure 2. Through-Via Resistance Distribution

Figure 3 shows the 10-mil daisy chain resistance distribution for each of the 20 panels. The resistances for panels numbered 16 and 19 are considerable greater than those of the other panels, account for the outside values indicated in Figure 2, and correspond to decreased conductor height for panels 16 and 19 shown in Figure 1. More importantly, the high resistance values in panels 16 and 19 indicate that the vias have much thinner copper than the vias in the other 18 panels.

Four of the 20 panels were subjected to an assembly simulation process to determine the robustness of the vias. Panels numbered 1 and 2, and panels numbered 16 and 19, with the lowest and the highest resistance values, respectively,

were selected from the two lots. Each of the four panels was processed six times through an infrared oven, alternating the side up in the oven on successive passes. The temperature profile for each pass included two minutes rise time to 183ºC, one minute dwell at solder reflow temperature (183-215ºC), and three minutes cool down to room temperature.

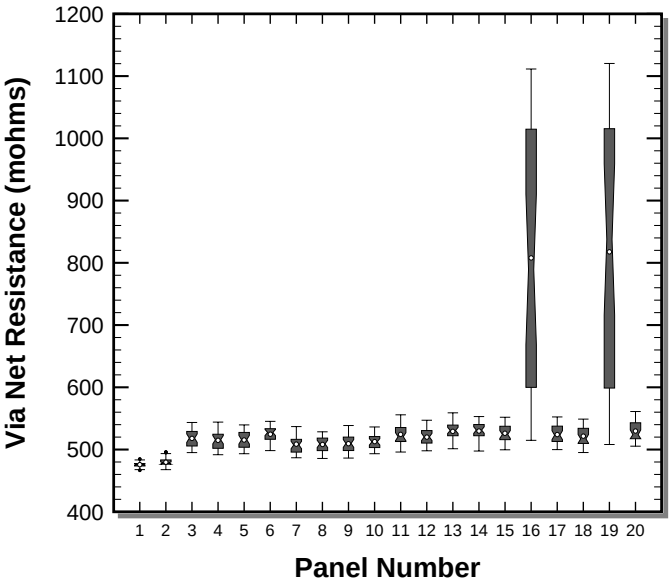

Figure 3. Through-Via Resistance Distribution by Panel (10-mil Diameter Via)

The results of assembly simulation are displayed in Figure 4, where the relative change in via net resistance for the 10-mil via is plotted for each stressed panel. Clearly, daisy chain resistances on panels numbered 16 and 19 changed significantly, compared to those of panels numbered 1 and 2.

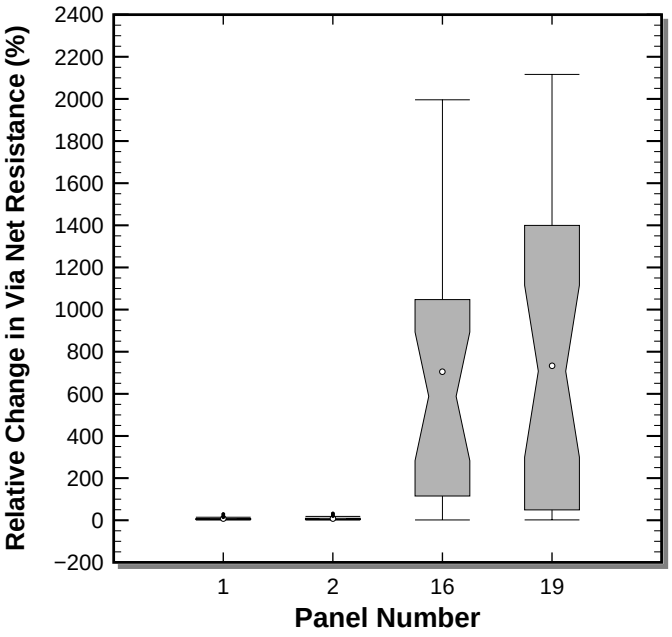

Figure 4. Resistance Change by Panel from Assembly Simulation Stress (10-mil Diameter Via)

Table 1 shows the resistance change statistics for the 10-mil vias in the four assembly simulation stressed panels. The table includes the number of daisy chain nets, and the mean, minimum, first quartile (Q1), median (Q2), third quartile (Q3), and maximum resistance changes for each panel. There were 29 through-via modules on each panel, initially with zero "open" nets. After the assembly simulation, six nets on panel 16 and 2 nets on panel 19 became "open", reducing their totals to 23 and 27, respectively.

Panel No.	No. Nets	Resistance Change (%)					
		Mean	Min	Q1	Q2	Q3	Max
1	29	7.4	1.1	3.6	5.6	7.9	29.4
2	29	7.9	1.0	3.6	5.5	9.5	32.2
16	23	705	1.5	115	588	1047	1995
19	27	733	1.7	49	707	1399	2116

Table 1. Resistance Change Statistics from Assembly Simulation Stress (10-mil Diameter Via)

The mean change in net resistance due to assembly simulation was 7.4, 7.9, 705, and 733 percent for panels 1, 2, 16, and 19, respectively. The maximum values for panels 1 and 2 (29.4 and 32.2 percent) were less than the first quartile values for panels 16 and 19 (115 and 49 percent).

Summary

As technology advances, feature sizes on printed circuit boards decrease – but become more difficult to manufacture. In addition, to achieve the necessary interconnection density, electrical performance, and reliability required of many products, the features must be manufactured to tighter specifications. Even when afforded the latest materials, equipment, and manufacturing processes, fabricators must implement controls to ensure that processes are repeatable.

In the example used in this and the previous column, poor control of copper plating resulted in large variations in outerlayer copper thickness and plating thickness in through vias. The problem that began in the plating process rippled through to subsequent processes, adversely affecting controlled impedance, via quality, and via reliability.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VII • Issue 12**

A CASE FOR COLLABORATIVE RESEARCH & DEVELOPMENT

The current economic recession has had a significant impact on the printed circuit industry. When supply exceeds demand, consolidation inevitably follows. We have seen the consequence of the recession in the form of layoffs, plant closings, plummeting PCB equipment and materials sales, and weak sales in the electronics sector in general.[1] As sure as night follows day, however, we will come out of the recession – but the North American PCB industry will have some lasting bumps and bruises. Some plants will remain closed, and many of the unemployed will have to find jobs elsewhere. Some manufacturing business will be lost to offshore fabricators permanently due to lower prices.

The basis of the present downturn is twofold – the world recession and the shift of high volume production of low and medium technology printed circuit boards to Asia.[2] Economics are the primary driving force leading to increased manufacturing in Asia, particularly China. Direct labor costs in Hong Kong are $7.58 per hour, less than half the direct labor costs incurred by PCB manufacturers in the United States. Direct labor costs in other regions in China (including Shanghai, Shenzhen, Guangzhou, Doumen, and Wuxi), however, are less than $1.00 per hour. When coupled with lower construction costs, tax incentives, subsidized loans, minimal environmental policies, and an enormous emerging market in China, the decision to manufacture PCBs in China is clear-cut.

Manufacturers of low and medium technology printed circuit boards fabricated in North America cannot compete with Asian fabricators on price. North American fabricators are offering low prices in an effort to cover their fixed costs, while operating at approximately 50 percent capacity.[2] Two niche markets are expected to provide protection to North American PCB fabricators: first, prototypes and low-volume high-mix designs with short lead times that can be fabricated by quick-turn shops, and second, high-volume high-technology circuit boards and back planes that require capability that is not widely available in Asia at this time. As new facilities ramp up in China, however, their capabilities to manufacture higher technology circuit boards will improve – further eroding the North American niche. The key for an extended North American PCB manufacturing presence is ongoing research and development.

For years, the strength of the printed circuit business in North America has been high technology – mass-produced high layer count, fine line, small-hole multilayer boards and back planes. However, we are playing catch-up in the blind via high density interconnect business. We cannot compete with the low cost of labor and relaxed environmental regulations in developing Asia. To maintain market share, North American fabricators *must* offer added value (albeit at higher prices) to the OEM/CEM/EMS community.

Added value is not free! The capability to provide added value in the past has come, in part, from significant investments in research and development. The future will require similar commitments – but from where will they come? Years back, when many printed circuit shops were captive, the owners (AT&T, IBM, Texas Instruments, to name a few) provided R&D funding to develop and implement new technology so that increased interconnection capabilities were possible. In the early 1990's, prior to unloading their factories, many large corporations entered into a collaborative research program, spearheaded by the National Center for Manufacturing Sciences (NCMS) with funding from the Advanced Technology Program (ATP) of the National Institute for Standards and Technology (NIST). The **Printed Wiring Board Interconnect Systems** program, spanning a five-year period from 1991 to 1996, consisted of big players including AT&T, Digital Equipment, Hamilton Standard, Texas Instruments, AlliedSignal, Sandia National Laboratories, Hughes Electronics, and IBM. The total cost of the project was $31.8 million[3,4] with ATP providing 40.6 percent, the U.S. Department of Energy providing 16.3 percent, and the industry participants providing the balance of 43.1 percent. Because a portion of the funding came from the government, the findings were made available the U.S. PCB fabricators after the completion of the project. More than 200 research papers were presented at conferences by project members, disseminating results to industry. Benefits credited to the project include a savings of $35.5 million[4] by avoiding duplication of effort among the participants. Further, 30 research tasks were accomplished that would not have been undertaken were it not for the collaborative research program.[4] The collaborative efforts led to the formation of Conductor Analysis Technologies, Inc., to commercialize measurement techniques that were developed under the NCMS program, and to provide ongoing improvements in PCB manufacturing capability and quality.

Research and development collaboration among PCB fabricators, their suppliers, and their customers can lead to technological advancements that will provide the added value needed to sustain PCB manufacturing in North America. Small- and medium-sized PCB fabricators need to join this effort to leverage R&D, and reap the benefits of collaborative research. For this effort to be successful, the electronics industry must adopt a long-term view, allocating funding for research and development when times are good to sustain the effort when times are bad.

Coordination is required among the players and someone needs to become the Champion – the IPC, National Electronics Manufacturing Initiative (MEMI), and NCMS come to mind as possible candidates. Each has experience working with government agencies, as government funding will be a necessary part of the effort. The project should identify specific areas where successful R&D will keep North American PCB fabricators in the forefront and sustain manufacturing for the future. The IPC and NEMI roadmaps, and the data from the IPC-PCQR^2 database can provide direction. Areas that continue to need improvements include plating, lead-free alternatives, microvia formation, cleaning, metallization, and patterning, narrow lines and spaces, registration, lamination, material handling/automation,

specialized dielectric materials, and costs. Essentially, the materials, equipment, and processes that provide increased functionality, quality, reliability, and efficiency while reducing cost will be beneficial to the North American industry.

The R&D effort should employ accepted experimental techniques to study alternative materials, equipment, processes, and technologies. The work should be divided among the participants to avoid duplication of effort – thereby reaping the benefits of collaboration. Intellectual property that is developed by the participants should provide protection to the participants for an extended period. Collaborative research and development is essential to maintain a viable PCB manufacturing presence in North America.

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[1] Mike Buetow, *Bad Signs*, **PC FAB**, December 2001, pp. 32-38.

[2] *The North American PCB Industry in Transition*, **CIBC World Markets**, October 22, 2001.

[3] Albert N. Link, *Early Stage Impacts of the Printed Wiring Board Joint Venture, assessed at Project End*, 1997.

[4] NIST 97-31, *Study Highlights ATP Project's Impact on $7 Billion Printed Wiring Board Industry*, December 8, 1997.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VIII • Issue 1**

FACTORY DESIGN AND AUTOMATION

In the last column, a case for collaborative research and development was discussed. Offshore competition, particularly from Mainland China, poses a significant threat to printed circuit manufacturing in North America. Economics are the primary forces that are causing the shift to Asia, and direct labor costs contribute considerably to the inequality.

One factor that can begin to offset direct labor costs between North America and Asia is productivity. If printed circuit shops could be run with fewer operators, engineers, and managers (fewer is better than none at all), each working more productively, then the disparity in direct labor costs between China and North America could be reduced. The burden, however, should not be directed at the operators to work harder to fabricate more circuits per unit time – an approach with limited potential. The solution lies in factory design and automation.

The ideal fully-automated factory could be described as a seamless operation with raw materials entering at one end of the facility, and *perfect* finished circuit boards shipping from the other end of the facility, without ever being touched by human hands. Designs are loaded into the computer system, which provides design rule checks, orders materials, schedules production, and at the same time produces and mails invoices. The materials travel the main path through the factory until they require specialized processes. Computer controlled tracking and routing diverts the materials to the appropriate substations, and upon completion provides access back to the main path. There would be no need for inspection, repair, rework, or touchup, because the automated processes in this ideal factory work perfectly, every time.

Science fiction…? Perhaps. However, if one starts with an ideal fully-automated factory concept, chances of achieving a high-quality manufacturing facility that lends itself to high productivity, improved quality, and greater profitability improve.

Real-world printed circuit manufacturing falls short of the picture described by the ideal facility. *Perfect* finished circuit boards may be possible every time if design rules incorporated 20-mil lines and spaces and 32-mil through holes in 62-mil boards, but today's feature set commonly includes 3-, 4-, and 5-mil lines and spaces, high-aspect-ratio through vias, blind microvias with strict registration requirements, and traces that require tight impedance control. These features cannot be manufactured perfectly every time with today's technology – but improvements can be made if equipment suppliers work towards increased automation at affordable prices.

Automation lends itself to many printed circuit manufacturing processes. Material-handling equipment, including conveyors, accumulators, stackers, and the like, linked by computer tracking and robotic controls are the first area to be addressed. While this type of equipment has been used for many years in the industry, next-generation material-handling equipment should bridge the gap from one process to the next. For example, a print-and-etch process for the fabrication of innerlayers could be designed from raw materials (the core) through imaging, developing, etching, stripping, inspection, oxide, and into the lamination stack-up area without intervention from humans. Accumulators in the stack-up area can hold innerlayers until the automated robot system is signaled by the computer system to build the stack-up for that design, and place it into the lamination press.

Improvements in quality may also be realized by eliminating defects caused by operators handling and transporting materials from one station to the next. As feature sizes become smaller and cores become thinner, however, material transport systems must be designed in such a way as to reduce the potential for introducing defects.

Chemical analysis and controls are the next area where automation can provide significant impacts. Real-time computer-controlled monitoring systems, designed to analyze chemical baths and provide automatic additions, can keep processes within specification and ensure the manufacture of quality product. Control systems must be responsive, to minimize the effects of a chemical addition to the bath while maintaining proper chemical activity. Regeneration of chemistries can provide increased lifetime, reduce the volume purchased, and lower the impact on the environment. Recycling spent chemistry can also be beneficial to the fabricator, the supplier, and the environment.

Cleanliness is another issue that is important to factory design and automation. Chemical areas are often filled with fumes that corrode the equipment, and affect the health and performance of the engineers and operators working there. Proper ventilation systems with scrubbers that clean exhausted air should be installed to minimize the effects of fumes. Equipment suppliers should use materials in their designs that can withstand not only the chemicals in their machines, but also any chemical that is used in the same processing areas. Regularly scheduled maintenance and good house keeping support cleanliness, and will help keep equipment running smoothly.

There are many reasons that explain why North American manufacturing jobs are being lost to Asian countries. Economics are one of the primary forces causing the withdrawal from North America. As jobs are lost, the technical expertise disappears as well, leaving purchasers of printed circuit boards with fewer homegrown sources.

To some degree, improvements in productivity can counterbalance the direct labor cost disparity between North America and Asia. Factory design and automation significantly impact productivity. Tax incentives in the form of accelerated depreciation, if implemented, would assist fabricators to offset the additional expense of automated equipment. By starting with an ideal fully automated factory concept, manufacturers of printed circuit boards can build a facility that provides high productivity, improved quality, and greater profitability.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VIII • Issue 2**

PCQR^2 INDUSTRY STATISTICS - INTRODUCTION

The IPC D-36 Subcommittee, titled "Printed Board Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard and Database" was formed in September 2000 [1] to develop an industry standard for process capability test panel designs, and to establish a database of test results from printed circuit board suppliers.[2] Since its inception, the subcommittee has developed a family of sixteen process capability panel designs, [3] and a database [4] of test results that demonstrate the capability, quality, and relative reliability of panels from participating suppliers. The database, which includes detailed performance statistics on each set of panels for each supplier, [5] is available to Original Equipment Manufacturers (OEMs) and Electronics Manufacturing Service (EMS) providers through an annual subscription fee. Also included in the database are industry statistics [6] that summarize performance of the industry at large, by reporting achievement in terms of quartiles. This abbreviated summary is available to the participating suppliers, as well as to the database subscribers.

Industry statistics collected from 6-, 12-, 18-, and 24-layer process capability panel designs will be presented in upcoming columns for:

- outerlayer conductor and space,
- 0.5- and 1.0-ounce innerlayer conductor and space,
- buried core conductor and space,
- through via formation, registration, and relative reliability,
- 1-, 2-, and 3-deep blind via formation, registration, and relative reliability,
- buried via formation and relative reliability, and
- twelve different controlled impedance structures including single-ended and differential configurations.

The industry statistics report includes the number of process capability panel submissions, the minimum, first quartile, median, third quartile, and maximum of the population for each feature type (conductors, spaces, vias, etc.), and feature size fabricated. Also included in the report are the mean, range, and standard deviation for each feature type and size.

Future columns dedicated to the industry statistics report will present the ongoing industry performance based upon quantitative data collected from standardized test patterns that are designed to reproduce features commonly designed into product. Each process capability panel design has a range of feature sizes that enables fabricators to determine their "comfort zone," and provides direction for improvement. Based upon their performance and position within the industry as indicated by the industry statistics report, fabricators can apply development resources to areas requiring improvement that will provide the greatest payback.

OEMs and EMS providers subscribing to the database can ensure product quality and on-time delivery of their products by matching technology requirements to their current supply base, and adding new suppliers that demonstrate capability, quality, and relative reliability required of their products. The data can also be used to establish and maintain design guidelines, and to develop road maps for the manufacture of future products.

With over 100 participants representing more than 75 companies on the D36 subcommittee, the IPC has established a mechanism that will streamline the supplier management process. The quantitative data collected from standardized patterns provides a common yardstick against which all fabricators can be measured. The data-driven results will benefit OEMs, EMS providers, and their suppliers by improving manufacturing capability, product quality, and product reliability.

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[1] **IPC WORKS 2000**, Miami Florida, September 9-14, 2000.

[2] Ronald J. Rhodes, "The Formation of the Printed Board Process Capability, Quality, and Relative Reliability Benchmark Test Standard," *Between The Conductors*, **CircuiTree**, July 2001, p 28.

[3] Ronald J. Rhodes, "PCQR^2 Design Library," *Between The Conductors*, **CircuiTree**, August 2001, pp 36-40.

[4] Ronald J. Rhodes, "PCQR^2 Database," *Between The Conductors*, **CircuiTree**, September 2001, pp 20-23.

[5] Ronald J. Rhodes, "PCQR^2 Process Capability Report," *Between The Conductors*, **CircuiTree**, October 2001, pp 48-51.

[6] Ronald J. Rhodes, "PCQR^2 Industry Statistics Report," *Between The Conductors*, **CircuiTree**, December 2001, pp 24-26.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VIII • Issue 3**

PCQR^2 INDUSTRY STATISTICS – OUTERLAYER CONDUCTOR AND SPACE

This is the second in a series of columns that are dedicated to the industry statistics collected by the IPC D-36 Subcommittee *Printed Board Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard and Database*. Outerlayer conductor and space capability, quantified by defect density, and outerlayer conductor width and height quality, quantified by the mean, standard deviation, and capability potential index, are reported. The data are the summary of 19 submissions to the database, and include results from 6-, 12-, 18-, and 24-layer designs. There are seven submissions from North America, two from Europe, and ten from Asia. Table 1 summarizes the database submissions that are included in the industry statistics at this time.

Design Designation	Number of Layers	Panel Thickness (inches)	Technology	Number of Submissions
IPC-007A	6	0.062	Medium	8
IPC-010A	12	0.062	High	3
IPC-012A	18	0.093	High	2
IPC-014A	24	0.125	High	6

Table 1. PCQR^2 Database Submissions

Capability and Quality

Part of every supplier management program implemented by Original Equipment Manufacturers (OEMs) and Electronics Manufacturing Service (EMS) providers should include methods to ensure that their suppliers have the *capability* to manufacture the designs with the *quality* consistent with their products. *Capability* in this context implies the ability to successfully form the features that are designed in the printed circuit board. Given that the features were successfully formed, *quality* establishes the degree to which they conform to specification.

While the price of bare boards is an important aspect considered by OEMs and EMS providers, considering price alone can lead to costly mistakes. For example, if a supplier has low or no capability to manufacture specific features included in a design, poor yields will lead to delivery delays that may cause the OEM/EMS provider to miss their market window. Further, if the quality of the features that are formed in the printed circuit boards is poor, the electrical performance of the assembled circuit may be marginal – a problem that can be very expensive to address after products have been shipped to customers.

By measuring the capability and quality of the supply base with industry-accepted standardized test patterns, OEMs and EMS providers can:

- Quantify their current supply base capabilities
- Find, screen, and select new PCB suppliers
- Ensure product quality and on-time delivery
- Align current designs to PCB suppliers
- Design for manufacturability
- Establish and maintain design guidelines
- Collect quantitative data for road maps

Suppliers participating in the PCQR^2 program obtain capability and quality information as well. By participating in the program, suppliers realize the following benefits:

- Quantitative data on process capability and quality
- Directions for process improvements
- Direct comparison to competitors
- Accurately-stated capabilities
- Data-driven road maps

Outerlayer Conductor and Space Capability

Industry capability for outerlayer conductors and spaces is summarized in Table 2. The table reports conductor and space defect density statistics for each outerlayer conductor and space width included in the four process capability panel designs fabricated to date. The minimum, first quartile, median, third quartile, and maximum defect density values are reported for each conductor and space width. Also reported are the mean, range, and standard deviation of defect density. The "count" reported in the table refers to the number of submissions having that specific feature size, and is population upon which the statistics are based.

Defect density is reported in *defects per million inches* of conductor or space. A defect density of zero is recorded when there were no defective features in the population, and is the desired value. Generally, defect density increased with decreased feature width for both conductors and spaces. In some instances, contradictions to this trend were due to changes in the population for each specific feature width. Minimum space widths were 3, 4, and 5 mils for the 0.062-, 0.093-, and 0.125-inch-thick high technology designs, respectively, while the medium technology 0.062-inch-thick design had a 5-mil minimum space width. The expected space defect density trend holds through the third quartile, but one or more of the 18 submissions with the 5-mil space performed much worse than all five of the submissions with 4-mil space, accounting for the discrepancy.

Outerlayer Conductor Quality

The quality of the outerlayer conductors fabricated by 19 suppliers presently in the database is summarized in Table 3. The statistics for the mean, standard deviation, and capability potential index are reported for conductor width and conductor height, showing the variation among the submissions.

The mean outerlayer conductor widths from each submission are used to calculate the minimum, first quartile, median, third quartile, maximum, mean, range, and standard deviation. The target conductor width was the as-designed width in the Gerber data. The median values and the mean values are very close to one another. Median widths were approximately 0.8 to 1.1 mils narrower than target values, while some suppliers provided conductors that were nearly 2.0 mils narrower than

target.

The next section in Table 3 shows the statistics for conductor width standard deviation. Low values of standard deviation are desired, leading to greater quality. Once again, there is a large distribution among the 19 suppliers. Minimum values ranged from 0.13 to 0.17 mils, median values ranged from 0.19 to 0.28 mils, and maximum values ranged from 0.38 to 0.56 mils.

The outerlayer conductor width capability potential index (Cp), reported in the next section of Table 3, is based on specification limits of ±20 percent about the target width. High Cp values, which are achieved with low standard deviations, correspond to higher quality. Cp generally decreases with decreased conductor width, primarily because of tighter specification limits associated with narrower conductors. The median Cp values are 2.76, 2.36, 1.52, 1.31, 0.94, and 0.73 for 8.0-, 7.0-, 6.0-, 5.0-, 4.0-, and 3.0-mil-wide conductors, respectively. In many instances, the desired capability performance index (Cpk) for a manufacturing process is 1.33 or greater. Since Cpk is always less than or equal to Cp, it is advantageous to have Cp values much greater than 1.33. If Cp of 1.5 is arbitrarily selected as acceptable, then the industry statistics show that 7- and 8-mil conductors could be manufactured by the first quartile suppliers and above. Further, using the same criterion, 6-mil conductors could be manufactured by the median quartile suppliers and above, 5-mil conductors by the third quartile suppliers and above, and 4-mil conductors by the very best of the suppliers. No supplier demonstrated the fabrication of 3-mil conductors to a Cp of 1.5.

Industry statistics for mean conductor height are shown in the next section of Table 3. The specification called for a minimum of 0.8 mils. All suppliers exceeded the minimum conductor height. The median conductor height was 2.11 mils, with a minimum of 1.09 mils and a maximum of 3.2 mils. The excessive range is caused in part by the need to metallize holes in panels of different thickness from 0.062 inches to 0.125 inches.

Large variation in outerlayer conductor height can cause problems in bare board fabrication and in the assembly process. Small standard deviations are preferred, and indicate higher quality. Shown in Table 3, conductor height standard deviation ranges from a minimum of 0.05 mils to a maximum of 0.46 mils, with the median at 0.15 mils.

Outerlayer conductor height Cp is the last attribute listed in Table 3. The specification limits used to calculate Cp for outerlayer conductor height are ± 0.4 mils. Higher values for Cp correspond to higher quality. Conductor height Cp ranged from a minimum of 0.29 to a maximum of 2.8, with a median of 0.89.

Summary

The IPC D-36 PCQR^2 Subcommittee has developed a library of process capability panel designs, and a database of test results that demonstrate the capability and quality of fabricators. In addition to detailed reports on each submission, the database includes process capability data and industry statistics that provide a direct statistical comparison among submissions and a concise summary of industry performance at large, respectively. Details on the PCQR^2 program are available at www.pcbquality.com.

In this column, industry statistics for outerlayer conductor and space capability, and outerlayer conductor quality are summarized. Outerlayer conductor and space capability is characterized by defect density, while conductor quality is characterized by the mean, standard deviation, and capability potential index for both width and height. The results show a wide range in performance among the 19 submissions currently in the database.

The PCQR^2 program benefits both OEM/EMS providers and printed circuit board fabricators. OEMs and EMS providers subscribing to the database gain valuable information that can streamline the supplier management process. Fabricators gain quantitative data about their manufacturing process that can be used for comparison against competitors, to apply resources for improvement, and to accurately state their capabilities in marketing campaigns.

Process Attribute	Width (mils)	Count	Min	Q1	Median	Q3	Max	Mean	Range	Std. Dev.
Conductor Defect Density (Defects per Million Inches)	3.0	11	38	82	735	3161	6057	1673	6019	2081
	4.0	11	0	15	47	208	2829	370	2829	835
	5.0	18	0	0	17	88	1072	120	1072	260
	6.0	19	0	0	0	76	848	96	848	204
	7.0	8	0	0	35	78	174	52	174	62
	8.0	8	0	26	35	79	315	74	315	103
Space Defect Density (Defects per Million Inches)	3.0	3	757	9161	17564	31257	44949	21090	44192	22306
	4.0	5	59	385	519	2399	3580	1388	3521	1529
	5.0	18	0	47	353	817	37826	2724	37826	8829
	6.0	16	0	35	106	406	1094	280	1094	356
	7.0	14	0	37	71	265	1563	237	1563	410

Table 2. Outerlayer Conductor and Space Capability

Process Attribute	Width (mils)	Count	Min	Q1	Median	Q3	Max	Mean	Range	Std. Dev.
Mean Conductor Width (mils)	3.0	11	1.55	1.77	2.12	2.31	2.91	2.10	1.36	0.41
	4.0	11	2.61	2.79	3.18	3.40	3.99	3.15	1.38	0.42
	5.0	18	3.01	3.84	4.06	4.37	4.96	4.09	1.95	0.47
	6.0	19	4.02	4.77	5.00	5.35	5.92	5.05	1.90	0.50
	7.0	8	5.01	5.78	5.97	6.18	6.77	5.96	1.76	0.61
	8.0	8	6.01	6.74	6.94	7.18	7.74	6.94	1.73	0.60
Conductor Width Standard Deviation (mils)	3.0	11	0.17	0.22	0.28	0.30	0.39	0.27	0.21	0.07
	4.0	11	0.17	0.22	0.28	0.33	0.38	0.28	0.21	0.08
	5.0	18	0.14	0.19	0.26	0.33	0.56	0.27	0.42	0.11
	6.0	19	0.13	0.19	0.26	0.33	0.55	0.27	0.41	0.10
	7.0	8	0.14	0.19	0.20	0.29	0.54	0.26	0.41	0.14
	8.0	8	0.14	0.19	0.19	0.28	0.56	0.26	0.42	0.14
Conductor Width Cp	3.0	11	0.52	0.66	0.73	0.93	1.15	0.79	0.63	0.22
	4.0	11	0.70	0.81	0.94	1.26	1.55	1.04	0.85	0.31
	5.0	18	0.60	1.01	1.31	1.74	2.44	1.38	1.84	0.48
	6.0	19	0.73	1.23	1.52	2.11	2.98	1.66	2.25	0.57
	7.0	8	0.86	1.64	2.36	2.50	3.47	2.13	2.61	0.82
	8.0	8	0.95	1.99	2.76	2.78	3.91	2.44	2.96	0.93
Process Attribute	**Spec. (mils)**	**Count**	**Min**	**Q1**	**Median**	**Q3**	**Max**	**Mean**	**Range**	**Std. Dev.**
Mean Conductor Height (mils)	0.8 Minimum	19	1.09	1.74	2.11	2.41	3.20	2.10	2.11	0.52
Conductor Height Std. Dev. (mils)	-	19	0.05	0.11	0.15	0.24	0.46	0.19	0.41	0.11
Conductor Height Cp	-	19	0.29	0.55	0.89	1.19	2.80	0.95	2.51	0.57

Table 3. Outerlayer Conductor Quality

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VIII • Issue 4**

PCQR^2 INDUSTRY STATISTICS – HALF-OUNCE INNERLAYER CONDUCTOR AND SPACE

Continuing the discussion of the industry statistics collected by the IPC D-36 Subcommittee *Printed Board Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard and Database*, this column presents the results from half-ounce innerlayer conductors and spaces. Innerlayer conductor and space capability are quantified by defect density, and innerlayer conductor width and height quality are quantified by the mean and capability potential index. The data are the summary of 25 submissions to the database, which include results from ten medium-technology 0.062" 6-layer designs, four high-technology 0.062" 12-layer designs, one medium- and two high-technology 0.093" 18-layer designs, and eight high-technology 0.125" 24-layer designs. There are seven submissions from North America, two from Europe, and 16 from Asia.

Half-Ounce Innerlayer Conductor and Space Capability

Industry capability for innerlayer conductors and spaces is summarized in the first section of Table 1. The table reports conductor and space defect density statistics for each half-ounce innerlayer conductor and space width included in the database. The minimum, first quartile, median, third quartile, and maximum defect density values are reported for each conductor and space width. The "count" reported in the table refers to the number of submissions having that specific feature size, and is the population upon which the statistics are based.

Defect density is reported in *defects per million inches* of conductor or space. A defect density of zero is recorded when there were no defective features in the population, and is the desired value. For each conductor and space width, one or more fabricators were capable of producing defect-free features, while low defect densities were recorded for half the suppliers. Conductor and space defect density increased with decreased width for third-quartile submissions, while maximum values displayed the same trend but exhibited some exceptions. Defect densities for spaces were generally greater than that of conductors of equivalent width.

Half-Ounce Innerlayer Conductor Quality

The quality of the half-ounce innerlayer conductors from the current 25 database submissions is summarized in the remaining sections of Table 1. The statistics for the mean and capability potential index are reported for conductor width and conductor height, showing the variation among the submissions.

The mean half-ounce innerlayer conductor widths from each submission are used to calculate the minimum, first quartile, median, third quartile, and maximum among all submissions. The target conductor width was the as-designed width in the Gerber data. Minimum conductor width values were 0.36 to 0.55 mils narrower than target, and maximum values ranged from 0.17 mils narrower than target to 0.7 mils wider.

The half-ounce innerlayer conductor width capability potential index (Cp), reported in the next section of the table, is based on specification limits of ±20 percent about the target width. High Cp values, which are achieved with low standard deviations, correspond to higher quality. Cp generally decreases with decreased conductor width, primarily because of tighter specification limits associated with narrower conductors. The maximum Cp values were 1.41, 2.13, 2.86, 3.53, 4.11, and 4.81 for conductor widths 2 through 7 mils, respectively. The minimum values for Cp were less than or equal to 1.0 for all conductor widths.

Industry statistics for conductor height are shown in the last section of Table 1. Mean values ranged from 0.38 mils to 0.67 mils for nominal 0.7-mil-thick copper. Conductor height Cp ranged from 0.35 to 4.84.

Summary

The IPC D-36 PCQR^2 Subcommittee has developed a library of process capability panel designs, and a database of test results that demonstrate the capability and quality of fabricators. In addition to detailed reports on each submission, the database includes process capability data and industry statistics that provide a direct statistical comparison among submissions and a concise summary of industry performance at large. Details on the PCQR^2 program are available at www.pcbquality.com.

In this column, industry statistics for half-ounce innerlayer conductor and space capability, and half-ounce innerlayer conductor quality are summarized. The results show a wide range in performance among the 25 submissions currently in the database.

Process Attribute	Width (mils)	Count	Min	Q1	Median	Q3	Max
Conductor Defect Density (Defects per Million Inches)	2.0	13	0	0	31	569	778
	3.0	14	0	0	16	103	253
	4.0	25	0	0	0	64	316
	5.0	24	0	0	0	32	479
	6.0	11	0	0	0	16	225
	7.0	11	0	0	0	16	291
Space Defect Density (Defects per Million Inches)	3.0	13	0	112	161	532	950
	4.0	14	0	31	84	152	252
	5.0	24	0	0	0	95	289
	6.0	10	0	8	32	57	413
	7.0	11	0	0	33	33	416
Process Attribute	**Width (mils)**	**Count**	**Min**	**Q1**	**Median**	**Q3**	**Max**
Mean Conductor Width (mils)	2.0	13	1.45	1.68	1.76	1.92	2.35
	3.0	14	2.49	2.68	2.81	2.99	3.67
	4.0	25	2.61	3.34	3.65	3.82	4.70
	5.0	24	3.64	4.43	4.68	4.83	5.67
	6.0	11	4.64	5.08	5.34	5.61	5.83
	7.0	11	5.61	6.08	6.32	6.61	6.83
Conductor Width Cp	2.0	13	0.50	0.67	0.82	0.87	1.41
	3.0	14	0.55	0.88	1.13	1.30	2.13
	4.0	25	0.57	1.13	1.42	1.78	2.86
	5.0	24	0.71	1.43	1.76	2.20	3.53
	6.0	11	0.85	1.68	2.03	2.85	4.11
	7.0	11	1.00	1.98	2.33	3.34	4.81
Process Attribute	**Spec. (mils)**	**Count**	**Min**	**Q1**	**Median**	**Q3**	**Max**
Mean Conductor Height (mils)	0.7 Nominal	25	0.38	0.57	0.60	0.62	0.67
Conductor Height Cp	-	25	0.35	1.04	1.48	2.26	4.84

Table 1. Half-Ounce Innerlayer Conductor and Space Capability and Quality

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VIII • Issue 5**

PCQR^2 INDUSTRY STATISTICS – 1-OUNCE INNERLAYER CONDUCTOR AND SPACE

The *Industry Statistics*, a summary of information collected by the IPC D-36 Subcommittee *Printed Board Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard and Database*, illustrates the capability, quality, and reliability of the printed circuit board fabrication industry. The previous three columns introduced the industry statistics, and presented results for outerlayer and half-ounce innerlayer conductors and spaces. This column presents the results from 1-oz innerlayer conductors and spaces. The data are the summary of 26 submissions to the database, which include results from ten medium-technology 0.062" 6-layer designs, five high-technology 0.062" 12-layer designs, one medium-technology and two high-technology 0.093" 18-layer designs, and eight high-technology 0.125" 24-layer designs. There are seven submissions from North America, two from Europe, and 17 from Asia.

1-oz Innerlayer Conductor and Space Capability

Industry capability for 1-oz innerlayer conductors and spaces is summarized in the first section of Table 1. The table reports conductor and space defect density statistics for each conductor and space width included in the database. The minimum, first quartile, median, third quartile, and maximum defect density values are reported for each conductor and space width. The "count" reported in the table refers to the number of submissions having that specific feature size, and is the population upon which the statistics are based.

Defect density is reported in *defects per million inches* of conductor or space. Conductor defect density was zero across all widths for more than half the suppliers, while 33, 47, 68, 70, and 50 percent of the suppliers recorded zero defect density for 4- through 8-mil spaces, respectively. For those suppliers having "shorts" and "opens" defects, defect density was generally greater for narrower features, and greater for spaces than for conductors of equivalent width.

1-oz Innerlayer Conductor Quality

The quality of the 1-oz innerlayer conductors from the current 26 database submissions is summarized in the remaining sections of Table 1. The statistics for the mean and capability potential index are reported for conductor width and conductor height, showing the variation among the submissions.

The mean 1-oz innerlayer conductor widths from each submission are used to calculate the minimum, first quartile, median, third quartile, and maximum among all submissions. The target conductor width was the as-designed width in the Gerber data. Minimum conductor width values were 1.25 to 1.65 mils narrower than target, and maximum values ranged from 0.38 mils narrower than target to 0.21 mils wider.

The 1-oz innerlayer conductor width capability potential index (Cp) is based on specification limits of ±20 percent about the target width. High Cp values, which are achieved with low standard deviations, correspond to higher quality. Cp generally decreases with decreased conductor width, primarily because of tighter specification limits associated with narrower conductors. The maximum Cp values were 1.27, 1.71, 2.30, 2.78, 3.22, and 3.69 for conductor widths 3 through 8 mils, respectively. The minimum values for Cp were less than or equal to 1.0 for conductor widths 3 to 7 mils, and 1.15 for 8-mil-wide conductors.

Industry statistics for conductor height are shown in the last section of Table 1. Mean values ranged from 1.19 mils to 1.33 mils for nominal 1.4-mil-thick copper. Conductor height Cp ranged from 0.56 to 4.73.

Summary

The IPC D-36 PCQR^2 Subcommittee has developed a library of process capability panel designs, and a database of test results that demonstrate the capability and quality of fabricators. In addition to detailed reports on each submission, the database includes process capability data and industry statistics that provide a direct statistical comparison among submissions, and a concise summary of industry performance at large. Details on the PCQR^2 program are available at ***www.pcbquality.com***.

In this column, industry statistics for 1-oz innerlayer conductor and space capability, and 1-oz innerlayer conductor quality are summarized. The results show a wide range in performance among the 26 submissions currently in the database.

Process Attribute	Width (mils)	Count	Min	Q1	Median	Q3	Max
Conductor Defect Density (Defects per Million Inches)	3.0	15	0	0	0	56	305
	4.0	15	0	0	0	38	342
	5.0	25	0	0	0	40	619
	6.0	25	0	0	0	0	517
	7.0	10	0	0	0	0	0
	8.0	10	0	0	0	0	0
Space Defect Density (Defects per Million Inches)	4.0	15	0	0	85	301	573
	5.0	15	0	0	34	135	289
	6.0	25	0	0	0	40	223
	7.0	10	0	0	0	31	253
	8.0	10	0	0	21	41	255
Process Attribute	**Width (mils)**	**Count**	**Min**	**Q1**	**Median**	**Q3**	**Max**
Mean Conductor Width (mils)	3.0	15	1.75	2.43	2.51	2.74	3.16
	4.0	15	2.79	3.43	3.60	3.82	4.21
	5.0	24	3.35	4.19	4.44	4.65	5.17
	6.0	25	4.36	5.20	5.44	5.63	6.17
	7.0	10	5.36	6.06	6.25	6.41	6.63
	8.0	10	6.35	7.05	7.24	7.39	7.62
Conductor Width Cp	3.0	15	0.33	0.69	0.91	1.07	1.27
	4.0	15	0.44	0.89	1.18	1.39	1.71
	5.0	24	0.56	1.07	1.38	1.73	2.30
	6.0	25	0.66	1.32	1.69	2.05	2.78
	7.0	10	1.00	1.32	1.83	2.01	3.22
	8.0	10	1.15	1.49	2.11	2.33	3.69
Process Attribute	**Spec. (mils)**	**Count**	**Min**	**Q1**	**Median**	**Q3**	**Max**
Mean Conductor Height (mils)	1.4 Nominal	25	1.19	1.24	1.27	1.30	1.33
Conductor Height Cp	-	25	0.56	2.15	2.48	3.55	4.73

Table 1. 1-oz Innerlayer Conductor and Space Capability and Quality

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VIII • Issue 6**

PCQR^2 INDUSTRY STATISTICS – THROUGH VIAS

The *Industry Statistics*, a summary of information collected by the *IPC Printed Board Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard and Database*, illustrates the capability, quality, and reliability of the printed circuit board industry. The previous four columns introduced the industry statistics, and presented results for outerlayer, half-ounce, and 1-oz innerlayer conductors and spaces. This column presents the results from through vias. The data are the summary of 26 submissions to the database, which include results from ten medium-technology 0.062" 6-layer designs, five high-technology 0.062" 12-layer designs, one medium-technology and two high-technology 0.093" 18-layer designs, and eight high-technology 0.125" 24-layer designs. There are seven submissions from North America, two from Europe, and 17 from Asia.

Through Via Capability

The capability, quality, and reliability of through vias are summarized in Table 1. Registration capability and via formation capability, indicated by probability of breakout and defect density are the first two sections in the table, respectively. The minimum, first quartile, median, third quartile, and maximum probability of breakout and defect density values are reported for each annular ring and hole/land combination, correspondingly. The "count" reported in the table refers to the number of submissions having that specific feature size, and is the population upon which the statistics are based.

Registration capability ranged significantly among the suppliers in the database. The best suppliers demonstrated registration capability down to a 5-mil annular ring, while the poorest performers recorded probabilities of breakout from 64 percent at a 9-mil annular ring to 100 percent for 4-mils and below. The median of the suppliers in the database recorded breakout for all annular rings, with the probability of breakout generally increasing with decrease annular ring sizes.

One-quarter of the suppliers produced defect-free vias down to drilled hole diameters of 12 mils, while half the suppliers produced 13.5-mil-diameter and larger vias without defects. No supplier produced defect-free 8-mil-diameter vias. At the other end of the spectrum, defect levels were high, and generally increased with decreased hole diameters.

Through Via Quality

The quality of the through vias from the current 26 database submissions is summarized in the next section of Table 1. The statistics for via net resistance coefficient of variation (COV - standard deviation divided by the mean, expressed in percent) are reported for each hole/land combination in the process capability panels, showing the variation among the submissions. The minimum values for 10-mil and greater diameter vias were less than 2 percent, and the median values were less than 6 percent. One quarter of the suppliers produced vias with a COV greater than 6 percent, with the poorest performance ranging from 17 to 116 percent.

Through Via Reliability

Reliability of the through vias is assessed by subjecting the process capability panels to six passes through an infrared oven to simulate the assembly process. This test identifies infant mortality failures, and shows the relative performance among the suppliers' submissions. Precision resistance measurements of the daisy-chain nets before and after stress are used to determine both "opens" and the change in resistance due to stress. The last two sections in the table report this data.

Half the suppliers provided 10-mil and greater diameter through vias that withstood the assembly simulation stress without causing electrical open circuits; three-quarters of the suppliers survived the test without opens in 12-mil and greater diameter vias; no opens were recorded in 14.5 and 16-mil diameter vias. However, some 8- and 10-mil diameter vias failed the test for half and one-quarter of the suppliers, respectively.

The percentage of daisy chain nets that exceeded 10 percent increase in resistance (includes opens) due to stress, suggesting impending failure with further testing, is reported last in the table. Three quarters of the suppliers provided some 8- and 10-mil diameter vias that exceeded a 10 percent increase in resistance due to the thermal stress, while in the extreme case, a small percentage of the 14.5 and 16-mil vias and 24-to-51 percent of smaller diameter vias exceeded the 10 percent threshold.

Process Attribute	Annular Ring (mils)	Count	Min	Q1	Median	Q3	Max
Probability of Breakout (%)	3.0	15	20.7	42.5	88.3	96.7	100.0
	4.0	26	2.8	47.2	69.7	84.5	100.0
	5.0	26	0.0	18.7	42.8	66.5	99.4
	6.0	26	0.0	2.6	14.2	51.9	95.5
	7.0	26	0.0	0.1	5.1	33.8	87.5
	8.0	26	0.0	0.0	1.1	15.0	76.8
	9.0	11	0.0	0.8	3.5	39.4	64.3
Process Attribute	**Hole/land (mils)**	**Count**	**Min**	**Q1**	**Median**	**Q3**	**Max**
Defect Density (Defects per Million Vias)	8 / 18	6	25	60	177	380	737
	10 / 20	15	0	15	44	178	2947
	12 / 22	26	0	0	6	30	1013
	13.5 / 23.5	26	0	0	0	27	512
	14.5 / 24.5	19	0	0	0	17	173
	16 / 26	11	0	0	0	0	44
Coefficient of Variation (%)	8 / 18	6	3.13	3.99	5.84	6.81	99.67
	10 / 20	15	1.35	4.24	5.30	6.40	16.98
	12 / 22	26	1.53	4.35	5.86	7.51	116.45
	13.5 / 23.5	26	1.47	4.32	5.59	7.36	37.79
	14.5 / 24.5	19	1.46	4.78	5.75	8.53	24.94
	16 / 26	11	1.75	4.48	4.79	6.77	24.92
Yield Loss from Assembly Simulation (%) Threshold: Open	8 / 18	6	0.00	0.00	0.31	3.24	17.16
	10 / 20	15	0.00	0.00	0.00	1.13	4.60
	12 / 22	26	0.00	0.00	0.00	0.00	5.23
	13.5 / 23.5	26	0.00	0.00	0.00	0.00	4.09
	14.5 / 24.5	19	0.00	0.00	0.00	0.00	0.00
	16 / 26	11	0.00	0.00	0.00	0.00	0.00
Yield Loss from Assembly Simulation (%) Threshold: 10% Change in Resistance	8 / 18	6	0.00	0.71	2.96	6.51	51.48
	10 / 20	15	0.00	0.29	1.42	5.03	39.08
	12 / 22	26	0.00	0.00	0.00	1.30	27.33
	13.5 / 23.5	26	0.00	0.00	0.00	0.00	23.98
	14.5 / 24.5	19	0.00	0.00	0.00	0.00	1.52
	16 / 26	11	0.00	0.00	0.00	0.00	1.52

Table 1. Through Via Capability, Quality, and Reliability

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume VIII • Issue 7**

PCQR² INDUSTRY STATISTICS – SOLDERMASK REGISTRATION

The *Industry Statistics,*[1] a summary of information collected by the *IPC Printed Board Process Capability, Quality, and Relative Reliability (PCQR²) Benchmark Test Standard and Database*,[2] illustrates the capability, quality, and reliability of the printed circuit board industry. Previous columns introduced the industry statistics, and presented results from outerlayer conductors and spaces, half-ounce and 1-ounce innerlayer conductors and spaces, and through vias. This column presents the results from soldermask registration. The results are the summary of 29 submissions to the database, which include data from ten medium-technology 0.062" 6-layer designs, five high-technology 0.062" 12-layer designs, two medium-technology and two high-technology 0.093" 18-layer designs, and ten high-technology 0.125" 24-layer designs. There are eight submissions from North America, two from Europe, and 19 from Asia.

Function of Soldermask

Application of soldermask is one of the last processes in the manufacture of printed circuit boards, and therefore, occurs when labor, time, and materials have accrued significant investment into the product. The major function of soldermask is to prevent solder bridging and electrical shorts from occurring between pads, and between pads and traces during the assembly process. Additional benefits[3] of soldermask include: constraining solder flow to ensure that the proper amount of solder is available at each solder joint; protect the outerlayer circuitry from handling damage; provide an environmental barrier; fill the space between outerlayer conductors with a material of known dielectric constant; provide an electromigration barrier for dendritic growth; and provide an insulator between the external circuitry and components mounted on the surface.

Registration Requirements

Typically, openings in the soldermask are formed that are somewhat larger than the pad, and must be registered well enough so that the pad is free of soldermask. The thickness of the soldermask, the height of the copper pads and conductors, and the soldermask registration capability determine the clearance between the pad and soldermask opening. As circuit density increases, the registration requirements of soldermask become tighter. The current soldermask registration requirements[4] for revenue center of gravity technology are three mils, while state of the art requirements are two mils.

Soldermask Registration Capability Results

Soldermask registration capability results for the 29 PCQR² database submissions are summarized in Figure 1. The graph shows clearance yield plotted as a function of clearance for maximum, third quartile, median, first quartile, and minimum tier suppliers. The supplier that demonstrated the best registration capability recorded 100 percent yield at clearances of 2 mils and greater, while third-quartile suppliers recorded 92.2 percent yield at the 2-mil clearance, 97.2 percent yield at the 2.5-mil clearance, and 99.4 percent yield for the 3- and 3.5-mil clearances.

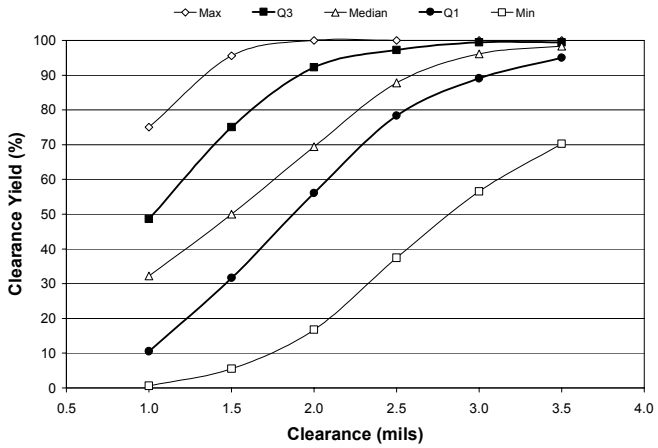

Figure 1. Soldermask Registration Capability

Revenue center of gravity includes the majority of high-volume printed circuit board manufacturing; therefore includes product from a minimum of first-quartile suppliers and above. Registration yield for first-quartile suppliers was 56.1, 78.3, 89.1, and 95.0 percent for 2-, 2.5-, 3-, and 3.5-mil clearances, respectively. Clearly, a gap exists between the soldermask registration needs of the industry and the registration capability of the industry.

The results show that some suppliers can meet today's registration needs, while others fall short. The needs of the industry will continue to become more demanding in the future. Those suppliers with inadequate soldermask registration capability must consider methods to make improvements – or be left behind.

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[1] www.pcbquality.com

[2] www.ipc.org/html/fsresources.htm

[3] Clyde F. Coombs, **Coomb's Printed Circuits Handbook, 5th Edition**, McGraw-Hill, New York, 2001, p34.2.

[4] IPC Technology Roadmap

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume IX • Issue 1**

TECHNOLOGY EROSION

For many years, the North American printed circuit board manufacturing community had maintained a technological advantage over their competitors in Asia, Europe, and other parts of the world. In recent years, however, we have seen an erosion of that superiority – to the point that many fabricators are fighting for their very survival. In this column, some of the causes of technology erosion are examined, and possible solutions are explored.

Factors Leading to Technology Erosion – a Brief History

During the 1970s and much of the 1980s, large vertically-integrated original equipment manufacturers (OEMs) owned much of the North American printed circuit board manufacturing capacity, and supported that business by applying significant research and development (R&D) resources to advance the technology. The OEMs complemented the R&D efforts of the materials and equipment suppliers to the industry, and together they developed processes to manufacture cost-effective printed circuit boards required at the time. As the global marketplace developed, independent shops without the heavy burden of R&D investment and the overhead of large OEMs could supply printed circuit boards at lower prices than the captive shops. The price-pressures created an overcapacity and underutilization situation in captive shops, and caused OEMs to cut overhead and R&D expenditures. Many captive shops became liabilities – unable to compete in the open market. Alternatives to much of the technology that OEMs' R&D dollars had developed were commercially available to others from the materials and equipment suppliers.

During the 1980s and 1990s, most OEMs sold off their captive printed circuit board businesses, arguing that printed circuit manufacturing was not their core business and printed circuits could be outsourced as a commodity. Research and development expenditures diminished as independent printed circuit board shops could not afford to make the investments required to continue the technological advancement trends of the past. Meanwhile, globalization continued, and printed circuit board manufacturing began to explode in Asia. Competing first with high-volume, low-technology designs, core competence began to emerge in Asia. Fabrication shops in Asia began investing in the latest available technology, and applied some of their own R&D efforts to advance technology. By the turn of the century, fabricators in Asia were the leaders in blind via technology. With an eager workforce coupled with low costs due to government support, low wages, and relaxed environmental regulations, Asian fabricators continued to take market share from the North American stronghold. Extending from late 2001 to the present, the latest economic downturn has lead to additional overcapacity, and to the demise of additional printed circuit shops in North America. Indeed, price pressure from Asia – particularly China, has taken business away from North America, but that would not have occurred without the technological expertise necessary to manufacture printed circuits – and that expertise is increasing!

Impact

The global marketplace is not only influenced by the market pressures of supply and demand, monetary exchange rates, international trade agreements, and tariffs, but by political wrangling as well. Thus, while the near-term supply of printed circuits appears secure, there is uncertainty about the long-term supply, especially if the sources are within a specific region or worse yet, from a single country. As OEM and electronic manufacturing service (EMS) companies continue to establish printed circuit manufacturing and assembly operations in China, similar operations in North America will be shut down and the associated engineering and manufacturing expertise will be interrupted – if not lost forever. Unemployed operators, technicians, and engineers will find employment, but most will find it in other fields.

As the erosion continues, the mainstay of North America remains quick-turn prototype operations and high-technology, high-layer-count multilayer boards and back panels. Without a concerted effort, however, the high-technology products will follow consumer products to Asia, where technology is improving and prices are low.

An interruption of the supply chain could be devastating to OEM and EMS companies. Uninterrupted supply of military electronics is even more critical. Therefore, it is essential that some printed circuit fabrication shops, along with the technical expertise to manufacture leading-edge circuits, continue to operate within North America. What will keep it here?

Turnaround Measures

Capability, quality, reliability, price, and delivery determine the marriage between purchasers and suppliers of printed circuit boards. Clearly, Asia – particularly China, offers the lowest price. If they can fabricate printed circuit boards with the necessary quality and reliability, and deliver what is needed, then the decision is clear – they get the business. Some products require increased capability (e.g. fine lines, small high-aspect ratio through vias, small blind vias, high layer counts, large panel format, tight registration); increased quality (e.g. tight conductor width and impedance controls, tight plating requirements); increased reliability (e.g. extreme operation conditions, military applications, life/death applications); or fast delivery (e.g. quick-turn prototype applications). It is in these areas that price is not necessarily the overriding factor, and where North American printed circuit board fabricators can play a role. The key is to acquire and maintain the technological advantage necessary to satisfy the additional capability, quality, reliability, and delivery needs. The fabricators cannot achieve this expertise without help. Well-funded, long-term collaborative research and development among fabricators and OEMs is one approach that can lead to breakthrough technology – intellectual property that is owned jointly by the participants, and protected by trade secrets and patents that will help to turn around the technological erosion.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume IX • Issue 2**

THE IMPACT OF CONDUCTOR WIDTH ON CONTROLLED IMPEDANCE

As higher bandwidth becomes commonplace in communication, computer, test and measurement, and other applications, the need for controlled impedance traces will become more frequent, with designs requiring ± 10 percent, ± 7.5 percent, and perhaps even ± 5 percent impedance control. The major factors that influence impedance are dielectric constant, dielectric thickness, conductor width, and conductor height. Each of these parameters must be well controlled if fabricators are to achieve the target impedance with the precision required of the design. This column examines impedance results from surface microstrip structures formed on 30 process capability panels that were supplied by a fabricator for the IPC Process Capability, Quality, and Relative Reliability (PCQR[2]) Benchmark Test Standard and Database.[1]

Process Capability Panel

The six-layer process capability panel used in this example is an 18- by 24- by 0.062-inch design with conductor/space, via, and impedance modules.[2] Thirty process capability panels were fabricated in three lots, with ten panels per lot. Lot-to-lot processing variations revealed signatures that pointed to the source of excessive impedance variation. Of particular interest is the impedance variation observed in the surface microstrip structures coincident with outerlayer conductor width variations.

Results

The impact of conductor width on controlled impedance is illustrated in Figure 1, where the impedance of surface microstrip structures is plotted versus outerlayer conductor width. The impedance structure called for a nominal five-mil-wide conductor on the surface, which was referenced to a plane one layer below the surface. The outerlayer conductor width data was collected from 67 conductor modules that were patterned on the surfaces of each panel, not the actual widths of the traces in the eight impedance modules on each panel. The target width for these conductors was five mils as well. A total of 1909 conductor width measurements (reduced from 2010 due to opens and shorts) and 240 impedance measurements are included in the analysis.

The data are the results from 30 process capability panels fabricated in three lots of ten panels each, and portray the lot-to-lot variation. Lot number two exhibited the lowest impedances centered around 47 ohms, lot number three the highest impedances centered around 55 ohms, and lot number one centered around 49 ohms. The horizontal bars show the range in conductor width measured on each panel, the vertical bars show the range in impedance measured on each panel, and the circles are plotted at the average conductor width and average impedance for each panel. The line drawn through the data is a linear regression that is provided to show the trend – not to predict results of a model. The range in conductor width shown in Figure 1 more closely depicts process variation over the surfaces of the panels than the range in impedance, simply because there are many more conductor modules than impedance modules.

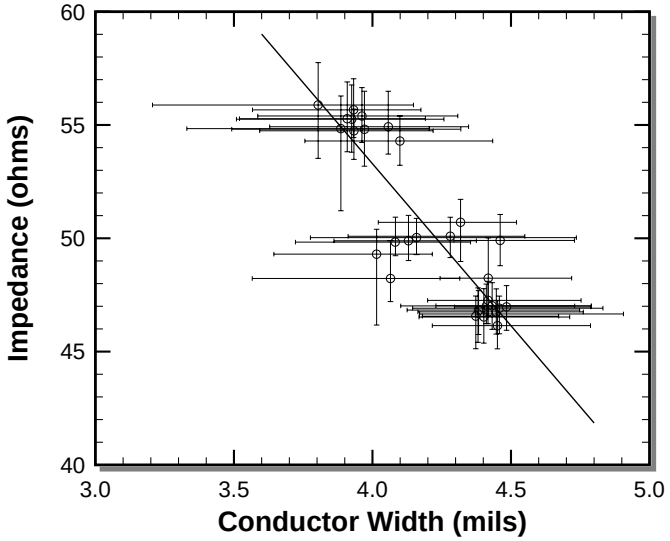

Figure 1. Surface Microstrip Impedance vs. Outerlayer Conductor Width

Discussion

The primary factors that establish the impedance of a surface microstrip trace are dielectric constant, dielectric thickness, conductor width, and conductor height. Thus, the variation in conductor width alone is not responsible for the range of measured impedance. Outerlayer conductor height, measured from the outerlayer conductor modules, ranged from a minimum of 1.45 mils to a maximum of 3.46 mils over the 30 process capability panels. Control of the dielectric constant and thickness is not known for these panels, but certainly impacted the impedance to some degree. Impedances were reasonably controlled within each of the three lots, but lot-to-lot variations contributed to excessive variation. This suggests that an understanding of lot-to-lot variation and process changes to minimize it would be prudent in an effort to improve the accuracy and precision of controlled impedance structures. Clearly, tighter control on conductor width and conductor height would lead to improved impedance control.

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[1] Visit www.pcbquality.com for details of the IPC PCQR[2] Subcommittee.

[2] Visit www.cat-test.info for details on process capability panels and the test modules.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume IX • Issue 3**

THE EFFECT OF INNERLAYER REPROCESSING ON CONDUCTOR HEIGHT

Innerlayer conductor height is often well controlled and slightly thinner than the nominal expected value. The nominal thickness for half-ounce copper, for example, is 0.7 mils, but conductors in finished circuit boards oftentimes measure approximately 0.6 mils in height. The precisions of the manufacturing processes that have been developed to produce electro-deposited foil allow venders to provide foils on the low side of the thickness specification. Further, fabrication steps such as the cleaning processes that are employed to enable the photoresist to adhere to the copper, and the oxide treatments that enhance the copper-to-epoxy bond in the finished board remove some copper from the surface. Together, these factors account for the deviation from nominal copper thickness.

The finished thickness of innerlayer copper traces is usually of secondary importance when compared to other parameters such as conductor width and the clearance between conductors. Unless taken to the extreme, thinning of innerlayers will have a small impact on the capability of the conductors to carry direct current or low frequency signals. Even in higher frequency designs, the thickness of the trace has a second-order effect on controlled impedance. It is perhaps for these reasons along with time and cost factors that fabricators reprocess innerlayers when conditions permit rather than scrap them.

Due to increased functionality within a smaller area and tighter impedance controls required in very high frequency applications, today's electronic circuits are more demanding then ever to fabricate. As conductors become narrower, tolerances must get tighter to achieve the desired functional requirements. Original Equipment Manufacturers (OEMs) and designers of printed circuit boards should be aware of the impact of innerlayer copper thickness variations on their products. To ensure signal integrity and product quality, the time has come to rethink the practice of reprocessing innerlayers.

Example Data

A set of 30 six-layer 0.062" by 18" by 24" process capability panels were submitted for testing and analysis and the results were included in the Process Capability Quality, and Relative Reliability (PCQR^2) Database.[1] The panels included outerlayer, half-ounce innerlayer, and one-ounce innerlayer conductor/space modules, through via registration and through via daisy-chain modules, and controlled impedance modules.[2]

Analysis of conductor/space data from the half-ounce innerlayers revealed five distinct copper thickness levels among the 30 panels. Figure 1 shows the mean half-ounce copper conductor height for each panel plotted versus number of processing cycles. The source of the variation was attributed to rework at the primary imaging step (strip photoresist, scrub, and reapply photoresist) or at the oxide treatment step (reprocess through oxide to eliminate oxide coating defects). There were eight panels that were processed once (normal processing), thirteen panels were processed twice, five panels processed three times, two panels processed four times, and two panels processed five times. The line drawn to the data is a least-squares liner regression with high correlation. The fit indicates that an average of 0.0875 mils of copper were removed per cycle, and that the average initial copper thickness was 0.687 mils.

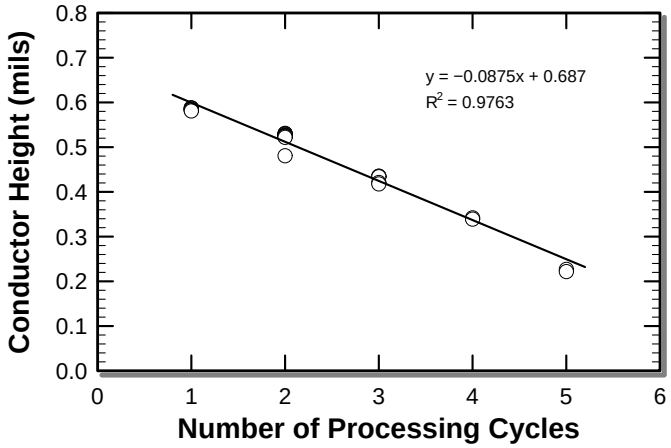

Figure 1. Conductor Height vs. Number of Processing Cycles for Half-Ounce Innerlayer Conductors

Discussion

Clearly, when a design calls for half-ounce copper innerlayers, conductors that measure 0.22 mils are too thin. Depending upon the uniformity of the process that removes the copper and the aggressiveness of that process, the thickness variation over the surface of the cores may grow with each cycle. The data presented here is the average for a panel; the minimum values were 0.010 to 0.059 mils thinner than average. Further, the total range (maximum thickness of all panels within a cycle minus the minimum thickness of all panels within the same cycle) exhibited an increasing trend with cycle, measuring 0.062 mils at the first cycle to 0.142 mils in the fifth cycle.

In some impedance configurations, a 0.2-mil decrease in trace thickness can result in a one to one-and-one-half Ohm increase in characteristic impedance. This error, on top of the distribution of impedances caused by variations in conductor width, dielectric spacing, and dielectric constant, can cause some panels to fail the controlled impedance specification. For critical high frequency designs that call for less than ±10 percent impedance control, fabricators should consider scrapping innerlayers, rather than reprocessing them. The cost of the innerlayer is small compared to a finished board that fails to meet the impedance requirements. On all other designs, one reprocessing cycle may be practical, provided it is acceptable to the fabricator's customer.

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[1] For additional information on the PCQR^2 program, visit www.pcbquality.com.

[2] For additional information on process capability panel designs, visit www.cat-test.info.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume IX • Issue 4**

IMPACT OF PANEL THICKNESS ON REGISTRATION

Through via registration intuitively becomes more challenging with increased panel thickness. Registration of vias with respect to patterned features on innerlayers of laminated multilayer panels depends upon the accuracy and precision of many processes including artwork plotting, imaging, drilling, and lamination. Registration tooling schemes (optical, mechanical pins, etc.) impact the final result as well. It is perhaps the lamination process including the stresses applied to the innerlayers that cause material deformation during high temperature and pressure that overwhelms the misregistration that occurs with increased panel thickness. In this column, registration results from the IPC-PCQR[2] database[1] illustrate the trends, and quantify the magnitude of increased misregistration that occurs with increased panel thickness.

Background

The data used to illustrate the impact of panel thickness on registration comes from 59 sets of panels (30 panels per set) submitted to the IPC-PCQR[2] database. The panels are 18 by 24 inches in size, with six registration modules on each panel: four at the corners and two near the middle.

Each registration module[2] consists of seven rows of through holes that are centered with respect to openings in copper patterns formed on innerlayers. Each row of holes has a different nominal clearance between the drilled hole and the innerlayer copper. Continuity measured between the copper pattern on innerlayers and the drilled and plated through hole indicates that the nominal clearance was exceeded, whereas an open-circuit measurement indicates that the misregistration was less than the designed clearance.

Results

Registration results are quantified by probability of failure, which is defined by the number of measurements achieving continuity divided by the total number of measurements, expressed in percent. Figure 1 is a graph that shows probability of failure plotted versus radial distance for a panel thickness of 0.031, 0.062, 0.093, and 0.125 inches, respectively. There was one set of panels that was 0.031-inches thick, 34 sets that were 0.062-inches thick, 13 sets that were 0.093-inches thick, and 11 sets that were 0.125-inches thick. The 0.031-inch panels were six-layer designs, the 0.062-inch panels were either six-layer or twelve-layer designs, the 0.093-inch panels were either twelve-layer or eighteen-layer designs, and the 0.125-inch panels were 24-layer designs. The data are median results for the industry. Thus, approximately half of the suppliers building panels of the thickness indicated performed better than the results shown, while the remainder performed as bad or worse than the results shown.

The data in Figure 1 show that additional registration allowance is necessary as panel thickness increases. For the industry median, a registration allowance of approximately one additional mil is required as panel thickness increases from 0.031 inches to 0.062 inches. Similarly, when panel thickness is increased from 0.062 inches to 0.093 inches, an additional one-mil allowance is required. A larger additional allowance is necessary when increasing panel thickness from 0.093 inches to 0.125 inches – approximately two mils.

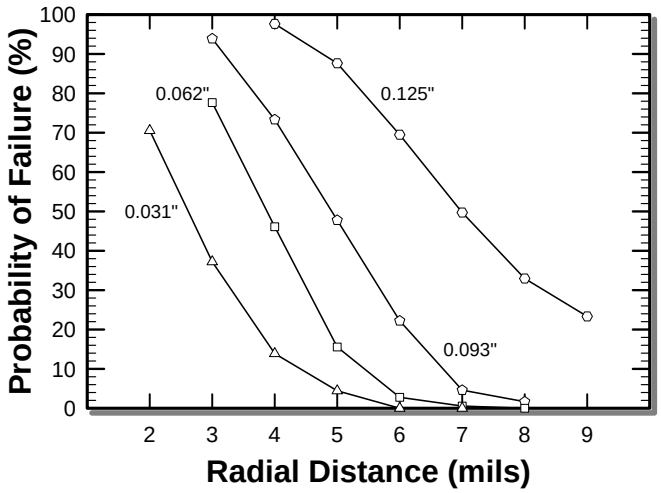

Figure 1. Median Through-Via Registration Results

A manufacturing process should operate at very low probability of failure, or perhaps zero probability of failure. Median suppliers in the industry operating under this premise would require six mils registration allowance for 0.031-inch-thick boards, seven mils allowance for 0.062-inch thick boards, eight mils allowance for 0.093-inch thick boards, and ten or more mils allowance for 0.125-inch thick boards.

Summary

Median through-via registration results from the IPC-PCQR[2] database illustrate the need for increased registration allowance as panel thickness increases. Increased registration allowance adversely impacts routing density. Because the data presented here is for the industry median with a wide range in performance among participating suppliers, designers of printed circuit boards must allow sufficient registration allowance so that designs can be manufactured by the industry at large, or purchasers of printed circuit boards must be discriminating in selecting the suppliers that are capable of manufacturing their products.

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[1] *Process Capability, Quality, and Relative Reliability Benchmark Test Standard and Database*, **IPC**. For additional information visit www.pcbquality.com.

[2] **Between The Conductors**, *Microvia Capability, Quality, and the Impact of Registration*, **CircuiTree**, April 2000, pp28-30. For additional information visit www.cat-test.info.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume IX • Issue 5**

A TOOL FOR PROCESS IMPROVEMENT

Fabrication of printed circuits involves complex multi-dependant operations that rely on the materials, equipment, and processes used in their manufacture. With so many possibilities, it's safe to say that there are no two complete manufacturing lines alike. The final results for completed printed circuit boards depend upon most, if not all of the following major steps: specific design, artwork, photoresist application, imaging, developing, etching, striping, laminating, drilling, plating, soldermask application and patterning, inspection, and test. Day-to-day changes within a given manufacturing line can, and often do, provide significantly different results. Chemical processes, for example, depend upon the concentration of ingredients, loading of the chemistry with the reactants, temperature of the materials, and delivery system. Fabricators sometimes compromise quality for throughput to improve equipment utilization. Increased acid concentration in an innerlayer line may allow a faster conveyor speed, but may provide poorer etching uniformity. Higher plating current densities may provide shorter process times, but the physical properties and uniformity of the copper may be compromised. Decisions like these are made every day by the management, engineers, and operators that run the day-to-day operations in the printed circuit facility.

It's difficult, if not impossible, to improve a process without first being able to measure it. Sometimes, fabricators use in-process yield or final yield to gage whether a process change is appropriate. While both in-process yield and final yield are important measures, they are dependant upon the specific design being manufactured – what's good for one design may not be good for the next. A better approach is to measure the electrical resistance of specific features to ascertain the impact of the process on the finished elements. After all, the metallic features are intended to carry electronic signals – what better way is there to characterize their quality? Now there is a tool that may be used to this end – namely a portable system that measures precision resistance, and can characterize the quality of conductors, vias, via registration, and soldermask registration.

Applications

There are many applications for which the portable system can be used. Suppliers participating in the IPC PCQR[2] program[1] have expressed a desire to collect data from process capability panels in the design library to optimize their processes prior to submitting panels for inclusion to the database. The portable system for process characterization and control can collect the data from most features in these designs and provide statistics that will point to areas that need development.

An extension of this application is in-line process monitoring and control. By incorporating one or more standardized test pattern modules[2,3,4] on a production panel, data can be collected from each part that is manufactured. Conductor width and height measurements could be collected at the end of the innerlayer etcher, for example, to assure that it has been set up properly. If conductor width is not within specification, adjustments to conveyor speed could be made before the complete lot is processed, leading to improved product quality.

Another application is to implement designed experiments to optimize processes, so that all product benefits from the changes. In a develop-etch-strip line, for example, one could study the impact that developer break point, developer chemistry, developer loading, and developer spray systems have on the defect density due to opens in conductors and shorts between conductors. After honing in on the optimal processing conditions for the developer, similar studies could be performed on the etcher to study conductor width uniformity. Examining each major process that impacts capability and quality provides a fundamental understanding of the process parameters and the knowledge necessary to implement permanent improvements.

Designed experiments can also lead to improved processes to form vias. Drilling, cleaning, and metallization processes can be examined to determine their impact on via yield and the resistance of via daisy chains. Only after the process is under control with consistent resistance readings for all daisy chains, is it appropriate to study reliability.[5]

Summary

Process capability and the quality of finished circuit boards varies significantly, depends upon the fabricator, and impacts the quality and reliability of the finished product. A new tool is now available to fabricators that acquires precision resistance measurements from specialized test patterns, and provides statistical results that may be used to optimize processes and improve product quality. The portable system for process characterization and improvement is used to measure manufacturing capability and product quality, providing the necessary data to make permanent improvements in the factory that lead to increased profitability.

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[1] Ronald J. Rhodes, ***Between The Conductors***, *The Formation of the Printed Board Process Capability, Quality, and Relative Reliability Benchmark Test Standard*, **CircuiTree**, July 2001, p. 28.

[2] Ronald J. Rhodes, ***Between The Conductors***, *Signatures from Conductor Process Capability Panels – Part V*, **CircuiTree**, January 2001, pp. 28-29.

[3] Ronald J. Rhodes, ***Between The Conductors***, *Microvia Capability, Quality, and the Impact of Registration*, **CircuiTree**, April 2000, pp. 28-30.

[4] Ronald J. Rhodes, ***Between The Conductors***, *Capability Study: Soldermask Registration*, **CircuiTree**, May 2001, pp. 68-69.

[5] Ronald J. Rhodes, ***Between The Conductors***, *Via Capability and Quality First - Then Reliability*, **CircuiTree**, March 2000, pp. 32-34.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume X • Issue 1**

Highly Accelerated Thermal Shock (HATS)

Over the past 30 years, the printed circuit manufacturing business has undergone a transition from predominately captive facilities that were owned by large vertically-integrated corporations to independent fabricators that served the commodity market. Once rich with research and development funding, the independents can no longer invest the resources on their own to make improvements in technology required for next-generation designs. Indeed, the materials and equipment suppliers today are providing much of the new technology to advance the industry.

Purchasers of printed circuits have many concerns when selecting fabricators to build their designs. Capability, quality, and reliability are primary factors to consider when making the selection. The IPC D-36 Subcommittee, *Printed Board Process Capability, Quality, and Relative Reliability Benchmark Test Standard and Database*, provides quantitative data on the manufacture of standardized patterns for Original Equipment Manufacturers (OEMs) and Electronic Manufacturing Service (EMS) providers to help ensure manufacturing capability, and the quality and reliability of their products. The database, which includes 111 submissions by more than 50 large printed circuit manufacturers over the past two years, reveals a wide range in manufacturing capability, reinforcing the need to be selective when sourcing designs for manufacture. If a fabricator lacks the capability to manufacture designs of specific (and required) complexity, delivery delays and unsatisfactory product quality will be certain, extending the time to market. Marginal product quality can lead to assembly problems and performance issues, especially in today's high-density, high-frequency products. Reliability is perhaps even more important to purchasers of circuit boards, especially in designs where circuit failures could jeopardize the lives of people using the products. Even without catastrophic failure, product returns can be very expensive, eroding profits and more importantly damaging the reputation of the OEM.

HATS™

Highly Accelerated Thermal Shock[1,2] (HATS™) is a new technology based on traditional air-to-air methods to evaluate the reliability of electronic interconnections within the circuit board and connections between the packages and the circuit board. The technique utilizes a single chamber that is alternately heated and cooled by an air stream that is forced past the samples. The unit is capable of temperatures from -60C to +160C. Thirty-six coupons (Figure 1), each with four daisy-chain nets, can be tested in one chamber load. Precision electrical resistances of each of the 144 nets are monitored during thermal cycling, providing data that shows the degradation of the nets during the test.

Test coupons are designed with software that is run from the Internet with a web browser. Coupon sizes range from a minimum of one-half by one inch to a maximum size of two by one inch. Designs can be created for circuits with two to eighty layers. Specific design parameters for each of the four daisy-chain nets include via type (through, blind, buried, or stacked), hole size, land size, interconnect track width, interconnect sequence, and grid size. Further, each net can include/exclude teardrops, non-functional lands, and soldermask coverage. Upon completion of the design process, the Gerber files are "zipped" and emailed to the designer. The design can be added to available panel area and manufactured with product, or placed on test panels to evaluate the reliability of alternative processes.

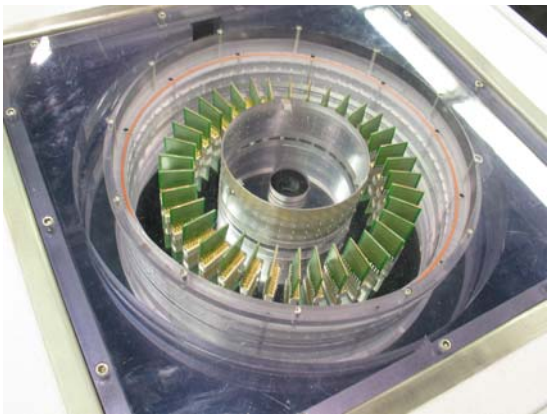

Figure 1. HATS™ Thermal Chamber with 36 Coupons

The coupons, on which connectors have been soldered, are inserted into the thermal chamber. The system is programmed and controlled by a personal computer running the Windows® operating system. A typical cycle time for a fully loaded chamber of 0.062-inch-thick coupons from -40C to +145C is six minutes. The HATS™ system provides data files that report the high and low resistance values for each net during each cycle. These data are read and processed by analysis software that creates tables and graphs of the results.

Discussion

The HATS™ system emulates traditional air-to-air techniques to impart thermal stresses upon the test samples. However, unique design features provide improved performance compared to traditional dual chamber methods. By alternately providing hot and cold air streams that flow across stationary samples, the electrical resistance of each daisy-chain net is easily monitored during the entire test, eliminating the need for long cables that must be moved from a hot chamber to a cold chamber and back again. Heat transfer to/from the samples is improved due to high volume forced convection air flow. The thermal mass of the chamber is minimized, providing for efficient heating and cooling of the samples. The result of these improvements is a shorter cycle time, in some cases cutting the time by more than a factor of four.[1]

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[1] Bob E. Neves, Rick B. Snyder, Timothy A. Estes, *Highly Accelerated Thermal Shock Reliability Testing*, **IPC Printed Circuits Expo®**, March 2003.

[2] Visit www.hats-tester.com for additional information.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume X • Issue 2**

HIGHLY ACCELERATED THERMAL SHOCK RESULTS

The previous column introduced a new method to study reliability of interconnections in printed circuit boards and solder joints between a package and the substrate upon which it is attached. This column presents results of thermal cycling tests performed on printed circuit boards.

As a part of the IPC *Printed Board Process Capability, Quality, and Relative Reliability Benchmark Test Standard and Database*[1,2] (PCQR^2) program, via coupons are subjected to thermal stress to ascertain their relative reliability performance. A database submission consists of 30 process capability panels that are manufactured in at least three separate lots. The process capability design[3] that was used in this particular test was an 18 by 24-inch, 12-layer medium-technology design that was 0.093 inches thick. Through via coupons had four daisy chain nets with 12, 13.5, 14.5 and 16-mil diameter holes, resulting in aspect rations of 7.75, 6.89, 6.41, and 5.81, respectively. Each net included 117 through vias with an interconnection sequence of 1-7-2-8-3-9-4-10-5-11-6-12.

One coupon was selected from each of six panels; two from the first lot of 10 panels, two from the second lot of 10 panels, and two from the remaining lot of the panels. Each coupon was subjected to six passes through a solder reflow oven to simulate soldering operations that printed circuit boards normally experience. On the last pass through the oven, a connector that is used to make electrical contact to the daisy chain nets was soldered onto the coupon.

After assembly simulation, the coupons were stressed in the Highly Accelerated Thermal Shock[4,5] (HATS™) test system. The temperature range, established by the PCQR^2 subcommittee, was -40C to +145C. The coupons were subjected to 500 cycles with a cycle time of approximately 10.6 minutes, and the entire test was completed in 89 hours. During the test, precision 4-wire (Kelvin) resistance measurements were made on each daisy chain net, at a rate of 28 readings per second. With a full chamber load of coupons (36 coupons having a total of 144 nets), the precision resistance of each net is sampled every 5 seconds. Both the high resistance and low resistance reading during each cycle are recorded for each net.

Figure 1 shows the results of the test for the daisy chain with the 16-mil diameter through hole. The graph shows change in resistance, plotted against cycle number. Change in resistance is referenced to the highest resistance recorded during the first cycle, and is calculated by:

$$100 * \text{resistance}[i]_{high} / \text{resistance}[1]_{high},$$

where i is the cycle number.

Three dashed lines are drawn on the graph for reference: one at y = 0, one at y = 5 percent, and the last at y = 10 percent. Each of the nets experienced very small change in resistance over the first 200 cycles. Beyond this point, a gradual increasing trend was observed, with two of the six nets changing abruptly and exceeding 10 percent change at 329 and 360 cycles, respectively. The earliest failure became an open circuit at 337 cycles, while the latter failure became open immediately at cycle 360.

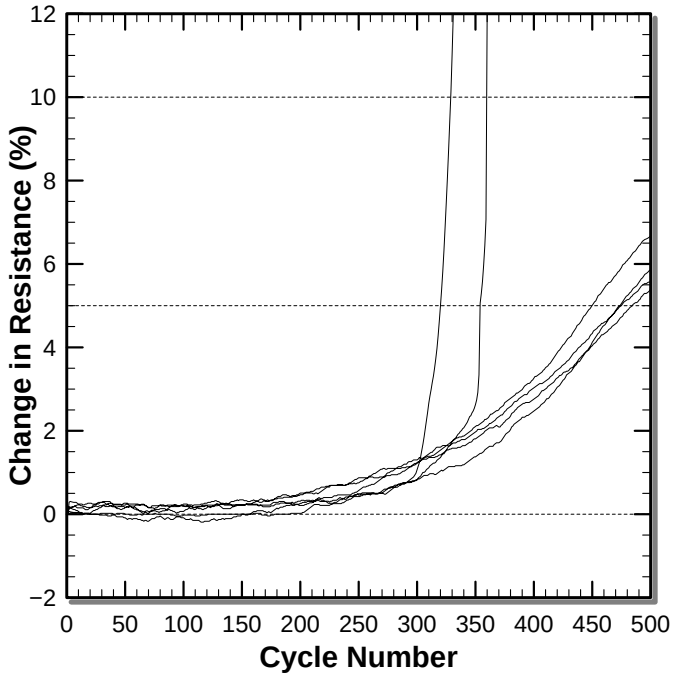

Figure 1. Net Resistance by Cycle: 16-mil Hole

The HATS methodology, adopted by the PCQR^2 subcommittee for relative reliability testing, is an economical, efficient, and effective technique to evaluate the robustness of printed circuit boards. In the example used in this column, two nets failed between 329 and 360 cycles, while four reached the end of the test with less than 10 percent resistance increase. This example is not typical of 12-layer submissions to the database – many submissions had much poorer performance, with early failures at assembly simulation or shortly thereafter. Thus HATS has provided relative reliability data that shows separation among the submissions to the database.

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[1] Ronald J. Rhodes, "The Formation of the Printed Board Process Capability, Quality, and Relative Reliability Benchmark Test Standard," *Between The Conductors*, **CircuiTree**, July 2001, p 28.

[2] Visit www.pcbquality.com for additional information.

[3] Ronald J. Rhodes, "PCQR^2 Design Library," *Between The Conductors*, **CircuiTree**, August 2001, pp 36-40.

[4] Bob E. Neves, Rick B. Snyder, Timothy A. Estes, *Highly Accelerated Thermal Shock Reliability Testing*, **IPC Printed Circuits Expo®**, March 2003.

[5] Visit www.hats-tester.com for additional information.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume X • Issue 3**

CONSUMER PRODUCTS

It's time for a change of pace… a break from the technical aspects of printed circuit board manufacturing to examine the philosophical mindset of consumer products. The world of consumer products has evolved over the years, and the telephone, for example, is one product that has a long history. In the days when AT&T was a regulated monopoly, the rotary telephone (some of you may remember the feature-poor but practical and reliable phone) was designed for 40-year life. Perhaps the overriding reason for such high quality was that the consumer did not own the phone – AT&T did. In those days, if a problem with the telephone occurred, AT&T had to send a service representative to the home to repair or replace it. Not so today! Loaded with features, today's phones are purchased by consumers, include a warranty of perhaps a year and often begin to fail shortly thereafter.

Consumer products are a high-volume, lower-cost, and sometimes – depending on market timing – a big profit margin business. Competition drives prices downward. For businesses in this field, innovative ideas brought to market in short design cycles can make all the difference. Controlling costs is essential for companies to maintain profitability; consequently, manufacturing has shifted from Europe and North America to Mexico, Japan, Singapore, and Korea, and most recently to China. Further, the enormous Asian market becomes available to those companies that establish manufacturing in the region.

Like other consumer products, telephones typically have a two-to-four year life before new features make them obsolete. Thus, the need to design for 40-year life is moot, but the throw-away mentality of consumer electronics has added a burden on landfills, and reinforced the environmental push for lead-free assembly. Planned obsolescence is a consequence of the free market economy, as competition among Original Equipment Manufacturers (OEMs) and Original Design Manufacturers (ODMs) calls for the development of new, smaller, faster, more powerful, more feature-rich products to satisfy their customers' insatiable appetite for the latest and greatest widgets.

Over the years there has been a plethora of new consumer products emerging from the electronics industry. Digital photography has become practical – even commonplace – as personal computers have advanced to the point where transfer, storage, manipulation, display, and printing of digital photos is affordable. It is not surprising that digital cameras have become a part of a cellular phone, offering yet another means of communication to the consumer. It is this type of innovation that keeps corporations in the limelight while maintaining a strong revenue stream. Many consumers who find this feature desirable will "retire" their current mobile phone early for one with a digital camera and other advanced features.

Advanced consumer electronics must be economical to manufacture, while providing the functionality, quality, and reliability that the consumer deserves – all at a reasonable price. Miniaturization, increased bandwidth, and environmental concerns impact the design and manufacture of consumer products. Miniaturization leads to smaller, more difficult-to-manufacture features (conductors, spaces, holes) on printed circuits, along with tighter registration requirements. Smaller features invariably lead to lower manufacturing yields, with increased costs associated with rework and scrap. Increased bandwidth requires that controlled impedance traces, which preserve signal integrity, are designed and fabricated in printed circuit boards. Once again, increased fabrication costs are associated with the requirements of controlled impedance. Environmental concerns and governmental regulations are requiring lead-free assembly processes. Because all lead-free assembly processes require higher temperatures than eutectic solder, it may be necessary to use high glass-transition FR-4 or perhaps even more expensive materials to withstand the assembly process. Furthermore, the reliability of the finished products may not be fully understood until considerable experience is gained with the specific materials and processes selected for lead-free assembly. Clearly, the pressures of miniaturization, increased bandwidth, and environmental concerns impact material, fabrication, and assembly costs of consumer electronic products.

The OEM/ODM community should be aware of the tradeoffs associated with advanced designs that push technology limits, especially when those decisions impact the bottom line. By utilizing design for manufacturability, the designer has the ability to create designs that can be manufactured by a larger base of fabricators. But where can designers get the information about fabricators' capability, quality, and reliability? The *Printed Board Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard and Database*[1] developed by IPC has the data. As the name suggests, the database includes capability, quality, and relative reliability data from a family of test pattern designs from two-to-thirty-six layers that mimic features on printed circuit board product. The database includes results from over 150 submissions with participating fabricators from Europe, North America, South America, and the Asia-Pacific region. Users of the database can benchmark their suppliers' capabilities, establish realistic design guidelines, ensure design for manufacturability, and select new suppliers – all leading to better designs and more intelligent sourcing. By taking advantage of the information in the database, electronics corporations can ensure the quality, reliability and timely delivery of their products to the marketplace.

[1] Visit www.pcbquality.com for additional information.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume X • Issue 4**

CAN WE BELIEVE THE POLLS?

The presidential election is over, and George W. Bush will remain President of the United States of America for another four years. Throughout the campaign, the print, television, radio, and internet media reported the results of opinion polls that were aimed at getting voters' impressions on campaign issues and on the candidates. Each of these so-called "scientific" polling processes asked the opinions of 1000 or so "likely" voters (sometimes "registered" voters) a number of questions about the economy and jobs, education, health care, prescription drugs, homeland security, and the war on terrorism. Given the sampling methods that were reportedly used by the pollsters, the margin of error was typically ±3 percent. In one poll leading up to the election that asked for whom would you vote, Senator Kerry and President Bush were deadlocked at 46 percent each, while another poll had the President ahead 50 to 44 percent. Which one should we have believed? Recognizing that the winner is determined by the Electoral College and not the popular vote, results of USA Today/CNN/Gallup polls were reported[1] in the battleground states of Florida (Kerry 49%, Bush 46%), Ohio (Kerry 50%, Bush 46%), and Pennsylvania (Kerry 46%, Bush 50%). All three polls were proven wrong – President Bush won in Florida and Ohio, and Senator Kerry won in Pennsylvania. Worse yet, exit polling that questioned individuals after they had voted showed "Kerry with a lead of three percentage points in Florida and four points in Ohio – both battleground states won by President Bush when the votes were actually counted."[2]

But what does this have to do with printed circuits? Important decisions should be based on reliable information. Fortunately, it is the count of the actual votes – not the pre-election or exit polls – that determine the outcome of an election. That's why we vote!

Procurement decisions for printed circuit boards are oftentimes based upon polling data. In some instances, procurers refer to fabricators' published design guides to determine if their design requirements can be met, or procurers often perform a shop audit and ask fabricators a series of questions regarding their manufacturing capabilities. What is your minimum line and space capability? What is the minimum diameter hole that you can drill and plate through a 0.093-inch-thick multilayer board? Can you hold ±10 percent on surface microstrip impedance traces? What is your registration capability for an 18-layer multilayer board? How accurately can you pattern soldermask?

Answers to these and similar questions rarely provide reliable information on which to base procurement decisions. The following may be more appropriate questions to ask the fabricator. What is your capability to form three-mil lines and spaces on innerlayers? What is the quality of the finished conductors, and how do you compare to your peers in the industry? What is your capability to form 12-mil through vias in 18-layer 0.093-inch-thick multilayer boards? What is the quality and reliability of the vias in the finished boards, and how do you compare to your peers in the industry? Can you show me the data?

Capability in the context of these questions implies the ability to form the features of interest, and may be quantified by statistical measures such as defect density: defects per million inches of conductor, defects per million inches of space, defects per million vias, and so on. Given that reasonable capability has been demonstrated, quality implies the accuracy and/or precision with which the features were formed, and may be quantified by statistical measures like standard deviation, coefficient of variation, capability potential index, and capability performance index. Once reasonable via formation capability has been demonstrated with acceptable quality, reliability of the vias may be assessed by subjecting samples to repeated thermal excursions between two extreme temperatures and reporting the number of cycles to failure. In this context, the relative performance of a group of fabricators may be assessed, and thus, the term relative reliability is appropriate.

There are still some unanswered questions. How do you compare to your peers in the industry? Can you show me the data? The answers to these questions require an industry standard. Comparison can only be made when each fabricator builds similar – if not identical – designs, and data are collected, analyzed, and presented in a consistent manner. Fortunately, IPC has developed such a standard, the *Printed Board Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard and Database*.[3] Members of the IPC D36 subcommittee have developed the IPC-9151A specification, which describes the test standard, and a family of test pattern designs that range from two layers to 36 layers. The process capability panels incorporate features that mimic those on product, but are designed to provide data that characterize the capability to form them, and their quality and reliability once they are formed. Specific features included in the designs are conductor/space, via daisy-chain, via registration, soldermask registration, and controlled impedance. Electrical tests are used to collect the data from the features, and statistical software is used to analyze the data to create reports, comparative data and industry trends.

Can we believe the polls? No – show us the data!

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[1] "Gallup Final Pre-Election Poll: Near-Deadlock," www.outsidethebeltway.com/archives/7854.

[2] "Bloggers Said to Blame for Bad Poll Info," The Associated Press, New York Times, November 4, 2004.

[3] For additional information visit www.ipc.org and www.pcbquality.com.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume XI • Issue 1**

THE GOOD, THE BAD, AND THE UGLY

Fabrication of printed circuits is *not* a trivial task! In fact, given the number of processing steps along with the vast array of materials used in their manufacture – not to mention that conductor widths are roughly the diameter of the human hair and through vias are three-to-six times that size – it's sometimes surprising that the finished products turn out as well as they do. While the price of the bare board is an important factor in the procurement of boards, a more important factor should be overall cost. In addition to the initial cost of the bare board, overall cost includes the cost associated with product delays because the supplier lacked the necessary capability to fabricate the specific design, the cost of rework and repair associated with poor quality, and the cost of product failures in the field associated with inferior reliability. The price of the bare circuit board is usually a small percentage of the finished product. Before adding those "expensive" components at assembly, it is prudent to ensure the quality and reliability of the bare circuit board.

The IPC PCQR[2] database[1] has been used by OEMs since 2001 to help in optimizing designs and making procurement decisions. In this Column, through-via data collected from a supplier database submission of thirty 12-layer 0.093-inch-thick process capability panels is discussed. Each 18-inch by 24-inch panel consists of 352 one-inch-square modules that cover the panel surface area. Module types included in the design are conductor/space, via registration, via daisy chain, soldermask registration, and controlled impedance. The through via daisy-chain results are enlightening – even shocking – and emphasize the value of the database.

The Good…

Each through-via module had four daisy-chain nets with 12-, 13.5-, 14.5-, and 16-mil diameter drilled holes, respectively. The land diameters were 10 mils larger than the drilled hole diameters, providing a 5-mil annular ring about the hole. Each net had 117 through vias with a layer interconnection sequence of 1-7-2-8-3-9-4-10-5-11-6-12. There were 28 through-via modules per panel, leading to nearly 400,000 vias in the 30-panel submission. The capability results from electrical test were good – not a single net was open and all vias were formed successfully.

The Bad…

The precision (4-wire) electrical resistances acquired from the daisy-chain nets were analyzed to determine the quality of the vias. Since each through-via module is identical in design, consistent resistances for each of the four nets are expected from tightly-controlled manufacturing processes, while large variations in resistance are characteristic of poorly-controlled processes. Variation can occur over the surface area of the panels as well as from panel-to-panel, and is often caused by plating and etching processes. The coefficient of variation (standard deviation divided by the mean, expressed in percent) is used to quantify quality. Good quality is indicated by coefficients of variation less than five percent. The quality results were bad – coefficients of variation were 10.9, 11.4, 12.3, and 13.3 percent for the 12-, 13.5-, 14.5-, and 16-mil vias, respectively.

The Ugly…

Six through-via modules were selected for HATS™ testing[2] to assess their ability to withstand the stresses that occur from thermal excursions. The test consists of 500 cycles with temperatures from -40C to +145C and provides reliability performance, relative to other submissions to the database. Prior to HATS, each coupon was subjected to six passes through an infrared oven to simulate the assembly process. On the last pass, a connector was soldered onto each coupon, which provided electrical access to each net during HATS testing. The precision resistance of each net was sampled every 10-to-15 seconds during the test, and the initial resistances were typically less than 1.0 ohm. A failure was indicated when a resistance increase of 10 percent was measured, and the daisy chain was considered "open" when net resistance exceeded 20.0 ohms.

The results were ugly! Two of the 12-mil nets and four of each of the 13.5-, 14.5-, and 16-mil nets were open (resistance greater than 20 ohms) after assembly simulation. Of the remaining nets that survived the assembly simulation process, the earliest 10 percent resistance increases were recorded at cycles 2, 1, 53, and 58 for the 12-, 13.5-, 14.5-, and 16-mil nets, respectively. Clearly, these samples were inferior to others that typically survive assembly simulation and last more than 100 cycles before the first failures are observed.

Significance…

Suppose that *your* responsibility was to secure 10,000 printed circuit boards for a new product that your company had developed. The time line was tight because your competitors had been developing similar products, and the first product to market can make significant profits. The boards were fabricated by the supplier that submitted the present samples to the PCQR[2] database and were delivered to the assembly plant on time – everything was on schedule. However, at final test and inspection, greater numbers of failures occurred than was commonly observed. You knew that something was wrong and began to investigate, but your company had to ship the product that passed functional testing or miss the window of opportunity. Although initial sales were good and profits began to roll in, your worst nightmare was realized as product failures were returned for replacement. The profits turned into losses, and your company's long-standing reputation for high-quality, reliable products suffered a blow. Could this happen to *you*?

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[1] The Printed Board Process Capability, Quality, and Relative Reliability Benchmark Test Standard and Database. Visit www.pcbquality.com for additional information.

[2] *Highly Accelerated Thermal Shock*, Integrated Reliability Test Systems, Inc., for additional information, visit www.hats-tester.com.

Between The Conductors

Conductor Analysis Technologies, Inc. **Volume XI • Issue 2**

STANDARDIZED PCB BENCHMARKING DATA – ONE CLICK AWAY

The Process Capability, Quality, and Relative Reliability (PCQR^2) Database[1,2] began in September 2000 when IPC formed the D-36 Subcommittee to establish a family of test patterns, a testing protocol, and a database that details the test results. The charter of the Subcommittee is to maintain a family of process capability panel designs utilizing the testing and data analysis techniques developed by Conductor Analysis Technologies, Inc., maintain a standard (IPC-9151) within the IPC family of process control documents, and maintain a database of PCB suppliers' capabilities. Since its inception, the PCQR^2 program has undergone substantial changes and additions. This column provides a brief update to the PCQR^2 program.

Subscribers

Currently there are 14 subscribers to the database:

- BAE Systems North America
- Delphi Corporation
- Honeywell International Inc.
- IBM Corporation
- Infineon Technologies AG
- Intel Corporation
- Lockheed Martin Corporation
- NASA
- Naval Surface Warfare Center - Crane Division
- Raytheon Corporation
- Rockwell Collins Inc.
- Sandia National Laboratories
- Teradyne Inc.
- Tyco Electronics Printed Circuit Group

The major business sectors represented by the subscribers include automotive electronics, desktop and mobile computers, low-, mid-, and high-level servers, test instruments, and defense and aerospace applications. The subscribers provide significant direction for the design of the test patterns, test methods, and results reported by the database. Access to the database allows subscribers to:

- Statistically benchmark board suppliers' capabilities
- Perform intelligent sourcing
- Select new suppliers
- Ensure design for manufacturability
- Establish realistic design rules

Suppliers

There have been 215 submissions to the database from 89 printed circuit board fabrication facilities as of April 2005. The majority of submissions have come from the Asia-Pacific region, with many from North America and Europe, and some from South America.

Suppliers receive detailed reports that document the results of their submission and compare their submission to the industry. The standardized test panel designs provide quantitative data on process capability, quality, and reliability that allows suppliers to accurately state their capabilities and provides a direct comparison to competitors. The reports pinpoint strengths and weaknesses in their processes, providing direction for allocating resources aimed at process improvements. Further, the reports provide data for establishing and maintaining road maps and design guidelines.

Process Capability Panel Designs

The family of test patterns has recently undergone its fourth revision, consolidating 26 designs down to 16 designs. The design matrix for the latest revision, which is summarized in Table 1, includes four types of designs:

- Rigid board
- Via board
- Package substrate
- Rigid-flex

The table lists the number of layers, design name, and elements within each design – indicated by a '√' or '●' in the table.

Table 1. PCQR^2 Revision D Design Matrix

# Layers	Design Name	CS	Via Registration						Via Formation								SR	Impedance	
			TV	1D	2D	3D	BB	SC	TV	BD	1D	2D	3D	BB	SV	BC	SC		SE	D
18" x 24" Rigid Board Designs																				
2	IPC-2R-D	√							√									√		
4	IPC-4R-D	√	√	√					√		√							√	√	√
6	IPC-6R-D	√	√	√					√		√							√	√	√
10	IPC-10R-D	√	√	√					√		√							√	√	√
14	IPC-14R-D	√	√	√					√		√							√	√	√
18	IPC-18R-D	√	√	√					√		√							√	√	√
18" x 24" Via Board Designs																				
10	IPC-10VA-D	●	√	√	√	√			√		√	√	√							
10	IPC-10VB-D	●	√	√	√			√	√		√	√					√			
14	IPC-14VA-D	●	√	√	√	√			√	√	√	√	√			√				
14	IPC-14VB-D	●	√	√	√			√	√	√	√	√				√	√			
24	IPC-24VA-D	●	√	√	√	√			√	√	√	√	√			√				
24	IPC-24VB-D	●	√	√	√			√	√	√	√	√					√			
24	IPC-24VC-D	●	√	√	√			√	√	√	√	√					√			
18" x 16" Package Substrate Designs																				
4	IPC-4P-D	√	√	√					√		√					√		√	√	√
6	IPC-6P-D	√	√	√			√	√	√		√			√	√	√	√	√	√	√
18" x 12" Rigid Flex Design																				
12	IPC-12RF-D	√	√						√									√	√	√

KEY:

CS	Conductor / Space	SV	Stacked Via
TV	Through Via	BC	Buried Core Via
BD	Back Drill Via	SC	Subcomposite Via
1D	1-Deep Blind Via	SR	Soldermask Registration
2D	2-Deep Blind Via	SE	Single-ended Impedance
3D	3-Deep Blind Via	D	Differential Impedance
BB	Blind Buried Via	●	Limited data for conductor height only

Testing

Four-wire precision resistance measurements are collected from conductor/space and via daisy-chain patterns, single-ended and differential TDR measurements from impedance patterns, and continuity measurements from registration patterns. After initial testing is completed, representative via coupons of each via type are extracted from the panels for reliability testing. These coupons are subjected to one of three unique assembly simulation profiles depending on the application:

- 215C max. (eutectic tin-lead)
- 245C max. (lead-free)
- 260C max. (lead-free)

After six assembly simulation cycles, the coupons are subjected to 500 Highly Accelerated Thermal Shock (HATS™) cycles[3] from -40C to +145C, while sampling the precision resistance of each daisy chain every 15 seconds.

Database

Flexibility and power have been added to the database, which consists of an interactive Microsoft® Excel workbook that contains results from all database submissions over the past two years. The subscriber may filter the submissions by design, material, and process criteria – thereby comparing submissions that are relevant to their application.

The IPC PCQR^2 program has evolved and grown since its inception in 2000, providing cost-effective, market-critical data to members of the electronics industry that leads to products with improved quality and reliability. The program will continue to grow while responding to Subcommittee members' needs and requirements… *Standardized PCB Benchmarking Data – One Click Away!*

[1] www.ipc.org
[2] www.pcbquality.com
[3] www.hats-tester.com