CAT is a provider of market-critical data utilized by designers, purchasers, assemblers, and manufacturers of printed circuit boards, and by material and equipment suppliers to the printed circuit industry. Our products and services provide quantitative data on printed circuit manufacturing capability, quality, and reliability.

Results from the analysis of CAT test panel and coupon designs provide quantitative yield,
uniformity and reliability data that are used to measure, track, and improve processes. Our data illustrate strengths and weaknesses of processes, and points to areas requiring improvement or development. Furthermore, the data offers insight into the sources of defects and process non-uniformities, allowing for their reduction or elimination.

CAT’s services include test panel and coupon design, precision electrical testing, reliability testing, and comprehensive data analysis. Whether measuring, comparing, or developing processes, we provide a standardized, independent, and documented evaluation of printed circuit board process capability, quality, and reliability.

The IPC PCQR² (Process Capability, Quality and Relative Reliability) Database, an extensive supply chain management resource, was developed by IPC and CAT in the fall of 2000 for designers, purchasers, assemblers and manufacturers of printed boards. It is based on statistical data collected from industry-developed test patterns that quantifies the capability, quality and reliability of printed board manufacturers.

PCB supplier facility benchmark data was first posted in the PCQR² Database in November 2001. Since then, 220 printed board supplier facilities have submitted one or more sets of test panels for evaluation yielding a total of more than 750 sets of test panels evaluated. Within the last 36 months, 78 different printed board supplier facilities have submitted one or more test panel designs for testing. There has been an average of 120 submissions recorded in the database over the rolling 36-month comparison period. By geographic region, the submissions over the last 36 months break down as follows: 70% from Greater China; 24% from North America; 6% from Asia/Pacific; and, 0% from Europe, Middle East & Africa.

OEMs and EMS providers can subscribe to the IPC PCQR² Database by paying an annual subscription fee. As part of that annual subscription, database subscribers have full access to all analysis reports generated from testing of each 15-panel submission from participating global PCB supplier facilities. The number of active database subscribers currently stands at 14. A total 32 different companies have subscribed to the database since its beginning.

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**CAT’S DAVID WOLF ON VIA RELIABILITY ANALYSIS**

**Figure 2: CAT analyzes all areas of the PCB for reliability.**
As part of the annual subscription fee, database subscribers can also sponsor up to 20 PCB supplier facility submissions during their 12-month subscription period at no additional cost.

Shaughnessy: Can you explain how you conduct a typical analysis of test panels and coupon designs?

Wolf: First, let me tell you about the PCQR² test panel designs. There are eight standardized test panel designs covering three levels of technology:

- Four single lamination designs with layer counts of 6, 10, 14 or 18 layers
- Two sequential lamination designs, either 14 or 24 layers, each with six different via structures
- Two HDI designs, both at 10 layers with either a 2+6+2 build-up construction or an any layer 4+2+4 stacked via construction

These process capability panel designs were developed by the IPC D-36 Subcommittee that oversees the IPC PCQR2 Database and are provided under license to IPC for use by its members and the printed circuit board community. The designs are to be used exclusively for the support of the IPC PCQR² Database. [Ed. Note: The design files for these test panel designs can be downloaded from this link.]

The designs incorporate the following structures in order to provide relevant statistics on the capability, quality, and reliability of the processes used in their manufacture:

- Outerlayer conductor/space capability
- Innerlayer conductor/space capability
- Via registration
- Via formation capability
- Via reliability
- Soldermask registration
- Single-ended controlled impedance
- Differential controlled impedance
- Conductive anodic filament
- Cross-section

All test data except controlled impedance is collected using precision resistance measurements. For impedance measurements, we use a robotic TDR tester.

CAT uses custom designed software to efficiently and accurately analyze test data and generate analysis reports and supplier facility comparison data.

Shaughnessy: You come across a variety of via structures. What sorts of trends are you seeing in via construction and associated via reliability? What’s the breakdown of mechanical vs. laser drilled?

Wolf: The standardized PCQR² test panel designs contain a variety of via structures which include: through vias; blind and buried microvias; buried via cores; multilayer sub-composite vias (both blind and buried); staggered and stacked microvias; and back-drilled vias. All eight of the standardized designs contain through via and 1-deep blind microvia structures using either two or four different drill diameters. The via structures and drill diameters used in the PCQR² test panel designs are dictated by the database subscribers through IPC’s D-36 Subcommittee. Thus, the database is good source for global PCB supplier via formation process capability and via reliability data.

With the increasing use of finer pitched ball grid arrays, 0.012” and 0.016” [0.3 and 0.4 mm] pitch, we are seeing an increase in the number and type of blind microvia structures with drill diameters at or below 0.004” [100 mm]. Blind microvias of this drill diameter and smaller are formed with laser drilling equipment. In the PCQR² test panel designs, multilayer through and sub-composite via structures with drill diameters of 0.006” [0.15 mm] and above are typically drilled with mechanical drills.

As an extreme example, the IPC-24VH-E sequential lamination test panel design has been built at a 0.187” [4.75 mm] thickness. With 0.010” [0.25 mm] drilled through vias, the result is an 18:1 via plating aspect ratio. There are global PCB supplier facilities who have successfully formed these high aspect ratio vias and who have also demonstrated via reliability (less than 10% change in via net resistance) after 6X convection reflow assembly simulation at...
a peak temperature of 260°C and 500 air-to-air thermal cycles from -40°C to +145°C.

We have collected via reliability data from many of the other standardized PCQR2 test panel designs that exhibit greater than a 5% change in via net resistance after the 6X convection reflow assembly simulation. May times those same via nets will not show failures (greater than 10% change in via net resistance) after 500 air-to-air thermal cycles; this due to the difference in z-axis expansion between +145°C and +260°C.

Another design trend that is becoming more common for higher layer-count boards, 14 layers and above, is the use of two-high (2+N+2) and three-high (3+N+3 or 3+N+N+3) staggered or stacked microvias on either side of multilayer sub-composite mechanically drilled vias. The unknown factor with these types of composite via structures is whether the stacked or staggered version is more reliable. The PCQR² database subscribers are requesting that these composites via structures be added to the next revision of PCQR² test panel designs so that via reliability benchmarking data can be collected. One major challenge with forming stacked via structures is registration during the sequential build-up of the via structures.

Shaughnessy: What are some of the more common via defects you see? How do blind/buried vias fare as far as defects?

Wolf: For through vias and sub-composite multilayer buried or blind via structures, the defects typically seen after assembly simulation and air-to-air thermal cycling are barrel cracks, knee cracks and/or inner layer separation. In blind microvia structures, whether staggered or stacked, separation of via hole plating from the target pad is a common defect. Generally, 1-deep (layer 1-2) and 2-deep (skip layer 1-3 with no interconnect on layer 2) blind microvia structures tend to be more reliable than high aspect ratio through or sub-composite via structures. This is due to less z-axis expansion associ-
ated with the smaller depth of the drilled hole and smaller plating aspect ratios.

**Shaughnessy:** What are your thoughts on back-drilled vias?

**Wolf:** Back-drilled via structures are common today in high frequency multilayer PCB applications. Back-drilling is used to remove that portion of a through via plated barrel without inner layer connections that would act as an antenna stub. Multiple depth back-drill via structures have been included in both the 14-layer and 24-layer PCQR² sequential lamination designs since January 2010. The reliability of back-drill via holes is very similar to through via holes of the same drilled diameter. The biggest challenge is drill depth control.

**Shaughnessy:** Are you seeing many landless vias, via-in-pad, or thermal vias?

**Wolf:** These types of via structures have not been part of the standardized PCQR² designs. The database subscribers have not specifically requested that these types of via structures be included in the test panel designs. With landless vias and via-in-pad, the major challenge is via registration.

**Shaughnessy:** What should PCB designers know about vias and via design?

**Wolf:** There are at least three areas of concern when evaluating the design of via structures:

A. Both via structure formation capability and uniformity must be controlled and repeatable before initiating via reliability studies. For the most reliable PCB designs, use the largest via drill diameter that the PCB design will allow; this yields the lowest via hole plating aspect ratio that is easier to process. With surface mount components that have a high number of pin-outs, staggered or stacked microvia structures might be required to successfully complete circuitry routing and interconnect requirements.

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**Figure 4:** Blind, through and stacked vias shown after thermal cycling.
C. There is a direct relationship between thickness and uniformity of plated copper in via holes and the ability to consistently form associated plated layer copper features that meet target width, space, diameter and height requirements.

PCB designs that contain high aspect ratio through vias, sequential lamination, and/or copper filled microvias can require multiple panel and/or pattern plating steps. Each plating pass adds to the thickness of the resultant copper patterns. Etching of thick plated copper is more difficult than thinner copper base foil or pattern plated foil. The variability in finished conductor width and height can have a direct influence on the ability to meet controlled impedance requirements.

Shaughnessy: Is there anything else you’d like to add?

Wolf: In 2013 CAT began using the OM Thermal Stress System to test both PCQR² and HATS™ via reliability coupon designs. The OM system is also capable of testing the AB/R and D coupon designs defined in IPC-2221B, Appendix A.

CAT developed the OM Thermal Stress System as a cost-effective performance based via net reliability test methodology which performs both convection reflow assembly simulation per IPC TM-650 2.6.27 and air-to-air thermal cycling per IPC TM-650 2.6.7.2 in the same test chamber with one set-up. Via net resistance measurements are continuously monitored with one reading taken per net every second.

Both the IPC PCQR² and the IPC-6012 QML programs utilize the OM system test methodology. The PCQR² program provides strong statistical data that quantifies process capability, quality and reliability while the QML program is a sampling plan which verifies conformance to IPC specifications. We offer the OM Thermal Stress Systems for sale or lease, and test services are provided from both CAT and our service partners.

Shaughnessy: Thanks for your time, David.

Wolf: Thank you. PCBDESIGN