UNDERSTANDING PROCESS CAPABILITY, QUALITY, AND RELIABILITY

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INTRODUCTION

Pressures to reduce package sizes and increase electrical performance have mandated technological developments in the design and manufacture of printed circuit boards (PCBs). Development efforts have been focused primarily on smaller feature sizes such as conductors, spaces, via-hole diameters, and via-pad diameters. As these features become smaller, they are inherently more difficult to manufacture, and because of increased circuit density, a greater number of vias and a greater length of conductors and spaces fit within the printed circuit board–manufacturing format. Therefore, smaller features must be fabricated at even lower defect densities than larger features to achieve equivalent yields.

Increased defect densities associated with smaller features along with the demands for greater electrical performance typically increase the price of the circuit boards. When manufacturing yields are lower than expected, delivery schedules are impacted, which may delay product introduction or even cause customers to miss market windows completely. Additionally, quality issues with printed circuits can cause a variety of problems during assembly, impact circuit performance, and ultimately result in product failure upon use by the end user.

Purchasers of printed circuit boards must manage the complexities of the technology, delivery, and price of boards that they are responsible for procuring while keeping in mind the capability of each of their suppliers and the quality of the boards they produce.

Circuit Density

The technology used to manufacture a printed circuit board is often determined early in the design process. The circuit designer works within the constraints of overall size, thickness, weight, electrical performance, and thermal demands, but may have discretion on parameters such as layer count, feature sizes, via structures, and material properties to achieve the design objectives.

Interconnect density is increased with narrower lines and spaces, and smaller diameter via holes and via pads. The major layer interconnect technology choices for multilayer board fabrication are through vias, blind vias, and buried vias. In many instances, all three technologies are incorporated into the finished board. High-density interconnect structures employ blind microvias to interconnect one or more layers without impacting routing on the

remaining layers. The ultimate reduction in via-pad diameter is illustrated in Figure 1, which shows a padless via.

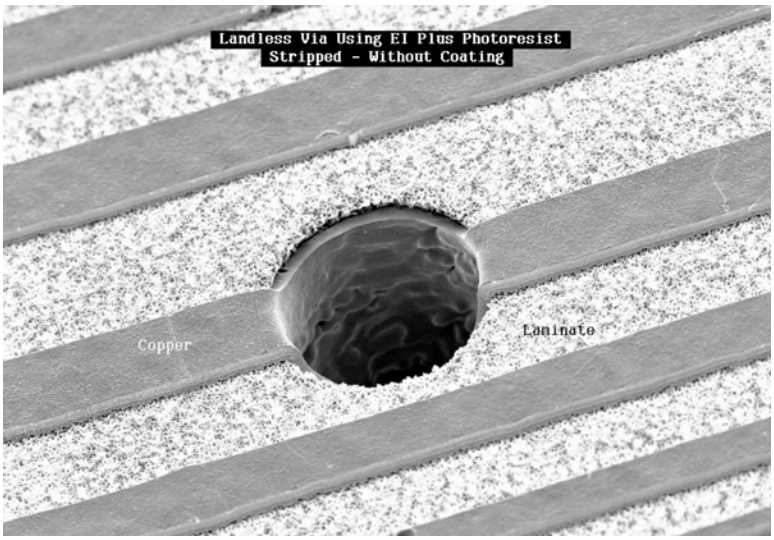

Figure 1. Padless via. (Photo courtesy of PPG Industries, Inc.)

Supplier Capability, Quality, and Reliability

Quantitative statistical measures that distinguish one supplier or process from another can assist procurement staff in decisions regarding supplier capability, quality, and reliability. Capability implies the ability to form features such as conductors, spaces, and vias successfully. Given that the features were formed successfully, quality refers to the degree to which they conform to specifications, and reliability describes their long-term performance due to environmental conditions.

By utilizing quantitative statistical measures, purchasers of printed circuits can minimize the potential of shipment delays caused by lower-than-expected manufacturing yields while ensuring the highest possible product quality and reliability.

Design for Manufacturability

Capability, quality, and reliability data collected from suppliers can be used to optimize designs for manufacturability. By minimizing or eliminating features that are difficult to manufacture, suppliers can produce designs at higher yields, lower costs, and improved quality and reliability, and with minimal risk of shipment delays. When designers follow predefined design rules based on supplier capability, quality, and reliability, both the purchaser and suppliers find themselves in a win-win situation.

MEASURING CAPABILITY, QUALITY, AND RELIABILITY

The approach to measure capability, quality, and reliability relies on three key elements:

- Specialized test patterns, referred to as process capability panels, designed to reproduce the features present in printed circuit boards

- Methods of testing the completed capability panels to extract raw capability, quality, and reliability data
- Data analysis techniques to generate relevant statistics

The printed circuit board manufacturing process can be represented by a transfer function (see Figure 2a). The input to the transfer function is the circuit board design data, typically Gerber data that contain design features, and the output is the actual printed circuit boards. The printed circuit board manufacturing process interjects defects and variations in the design features, which may be caused by material and process limitations, processing conditions, and process non-uniformities. When applied to process capability panels (see Figure 2b), the input contains a range of known design features, and the output is the capability, quality, and reliability data that are collected from the process capability panels.

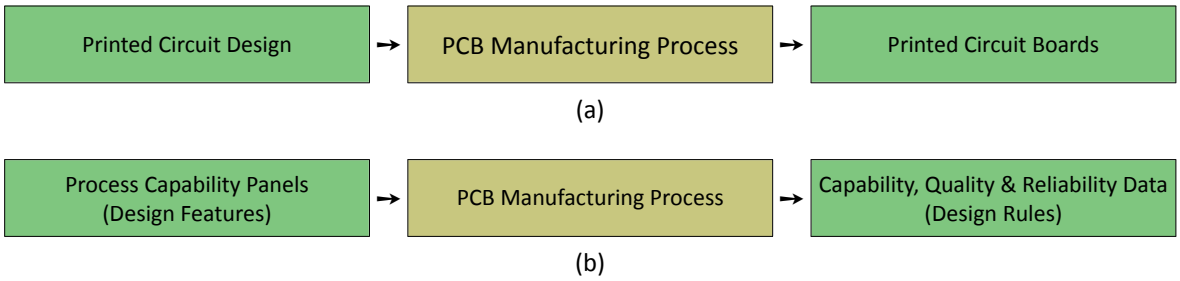

Figure 2. Capability, quality, and reliability measurement: (a) PCB manufacturing transfer function; (b) capability transfer function.

Process Capability Test Panels

The test patterns used to collect data from printed circuit board manufacturing processes should be designed conceptually as close as possible to the product that they are intended to model. This includes conductor and space sizes, via hole, pad and grid sizes, registration and impedance requirements, the number of layers, stack-up, board thickness, and materials.

A set of test patterns that have been specially designed to collect detailed process capability, quality, and reliability data on a range of feature sizes are shown in Figure 3. When distributed over the area of the manufacturing panel format and manufactured in sufficient numbers, they provide the basis for relevant statistics that depict the capability, quality, and reliability of the process that was used in their manufacture. Table 1 details the information that that can be obtained from each of these test patterns.

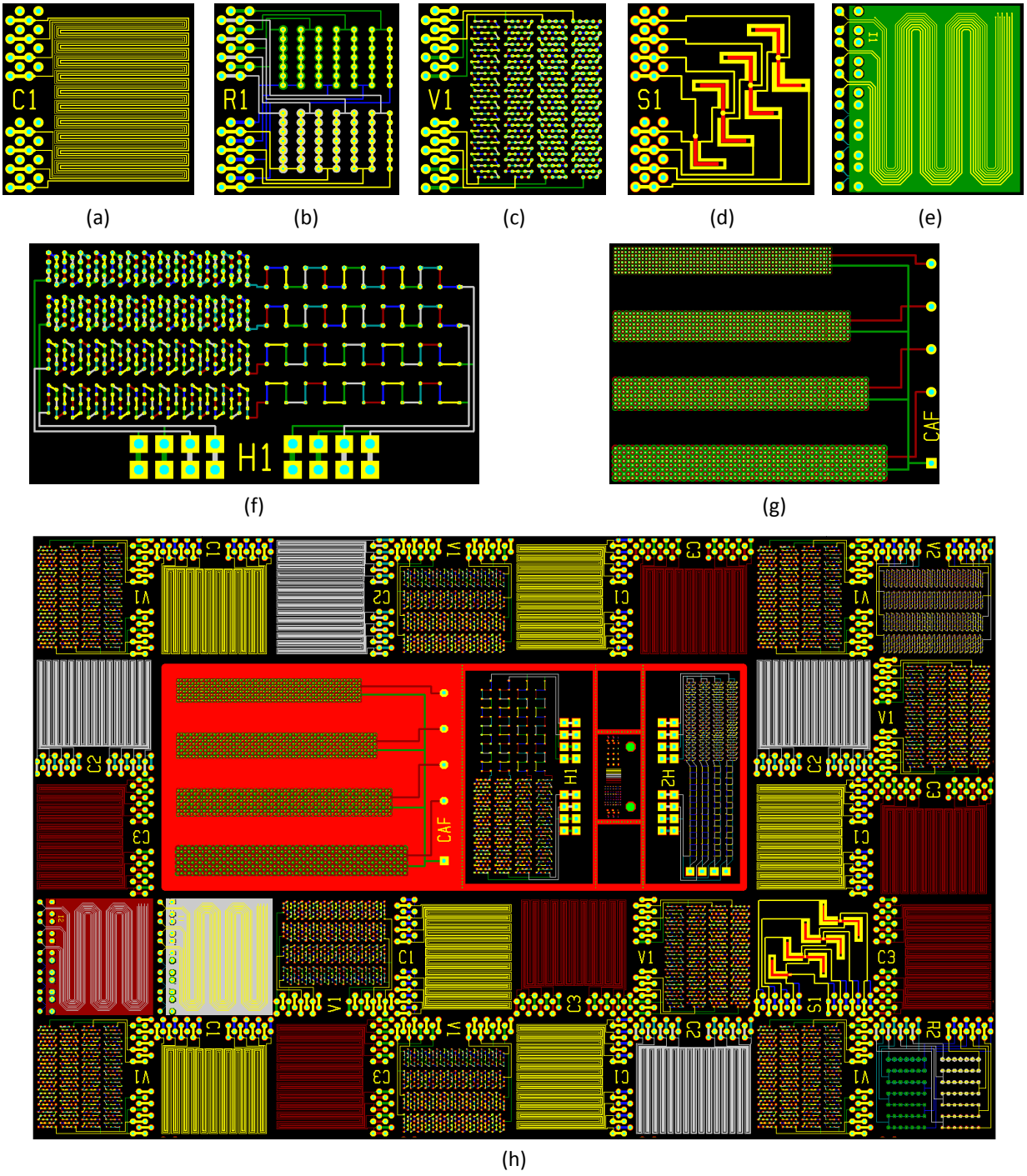

Figure 3. Specially designed test patterns for collecting detailed process capability, quality, and reliability data: (a) conductor/space module; (b) via registration module; (c) via formation module; (d) solder mask registration module; (e) controlled impedance module; (f) via reliability coupon, (g) conductive anodic filament coupon; (h) section of a process capability panel.

Module/Coupon	Capability	Quality	Reliability
Conductor/Space	Conductor and space yield	Conductor width and height control	-
Via Registration	Probability of breakout		-
Via Formation/Reliability	Via yield	Resistance control	Cycles to failure
Solder Mask Registration	Probability of encroachment		-
Controlled Impedance	Impedance control		-
Conductive Anodic Filament	-	-	Time to failure

TABLE 1. Test Pattern Statistical Attributes

Testing Methods

A variety of methods are available for collecting data from process capability panels. These include electrical (continuity, precision resistance, capacitance, inductance, time-domain reflectometry, etc.), optical (microscopy, x-ray, cross-sections, etc.), and other more specialized techniques. Regardless of the method employed, the data must be collected in a timely manner, and procedures must be established to ensure the accuracy and precision of the data.

DATA ANALYSIS TECHNIQUES

Defect Density

The calculation of defect density from capability data normalizes the probability of having defects and can be used to predict product yields. Defect density may be calculated for conductors, spaces, and vias. Eq. 1 is used to calculate conductor defect density from process capability panel capability data.

$$\lambda_C = \frac{-\ln\left\{\frac{Y}{100}\right\}}{l} \qquad \text{(Eq. 1)}$$

where

Y = conductor yield

l = length of individual conductors

λ_C = conductor defect density

Similar equations are used to calculate defect density for spaces and vias.

Predicted Yields

The fraction yield on product due to opens in conductors is calculated as shown in Eq. 2.

$$Y_{fo} = e^{-\lambda_C L_C} \qquad \text{(Eq. 2)}$$

where

λ_C = defect density of opens determined from process capability panels

L_C = total conductor length on product

Similarly, the fraction yield on product due to shorts between conductors is calculated by Eq. 3.

$$Y_{fs} = e^{-\lambda_S L_S} \qquad \text{(Eq. 3)}$$

where

λ_S = defect density of shorts determined from process capability panels

L_S = total space length on product

The product of the fraction yield due to opens and the fraction yield due to shorts provides an estimate of yield on product due to opens and shorts, as shown in Eq. 4.

$$Y_p = 100\, Y_{fo}\, Y_{fs} \qquad \text{(Eq. 4)}$$

Capability Potential Index

Control indices provide a numerical result that is indicative of the quality of features fabricated by a specific manufacturing process. The capability potential index, C_p (see Eq. 5), is the ratio of the difference between the upper specification limit (USL) and lower specification limit (LSL) to six times the standard deviation (σ). Larger capability potential indices indicate that the manufacturing process has greater potential to provide features that fall within the specification limits.

$$C_p = \frac{USL - LSL}{6\sigma} \qquad \text{(Eq. 5)}$$

Capability Performance Index

The capability performance index, C_{pk}, relates the mean and standard deviation to the specification limits by the relationship in Eq. 6. The capability performance index is always less than or equal to the capability potential index. If the mean (μ) is centered between the lower and upper specification limits, then the capability performance index equals the capability potential index; otherwise, it is less than the capability potential index. Larger capability performance indices indicate a greater probability of the data falling within the specification limits.

$$C_{pk} = \min\left\{\frac{USL - \mu}{3\sigma}, \frac{\mu - LSL}{3\sigma}\right\} \qquad \text{(Eq. 6)}$$

Coefficient of Variation

The coefficient of variation is defined as 100 multiplied by the standard deviation, divided by the mean (Eq. 7). This expression normalizes the spread in the data to the mean, and is sometimes called the relative standard deviation. For a given mean, smaller standard deviations characterize improved performance so that the smaller the CoV, the better.

$$CoV = 100\left\{\frac{\sigma}{\mu}\right\} \qquad \text{(Eq. 7)}$$

Probability of Breakout

Probability of breakout is a measure of the chance of a via hole being misregistered from its pad by a distance greater than the annular ring of the via. The probability of breakout is calculated for each designed clearance by Eq. 8.

$$P_{bi} = 100\left\{\frac{N_{fi}}{N_{ti}}\right\} \qquad \text{(Eq. 8)}$$

where

N_{fi} = the number of failures at clearance i

N_{ti} = the total number of opportunities at clearance i

Weibull Distribution

A Weibull distribution is often used for defects that occur over the course of time in field life data analysis. Equation 9 shows the general 2-parameter equation for the Weibull probability density function.

$$f(t) = \frac{\beta}{\eta}\left\{\frac{t}{\eta}\right\}^{\beta-1} e^{-\left\{\frac{t}{\eta}\right\}^{\beta}} \qquad \text{(Eq. 9)}$$

where

β = shape parameter

η = scale parameter

CONDUCTOR AND SPACE CAPABILITY AND QUALITY

The ability to manufacture conductors and spaces successfully, as measured by defect density, provides a convenient means to estimate expected yield on product, and illustrates the impact of defects on yield. Figure 4 shows predicted product yield due to opens and shorts plotted versus feature length for 3-, 4-, 5-, and 6-mil conductors and 4-, 5-, and 6-mil spaces formed on outerlayers. The curves show that for a fixed defect density, yield falls off with increased conductor length on product. At 33 defects per million inches of 6-mil conductor, predicted product yields (due to opens) for 100, 1000, and 10000 inches of conductor are 99.7, 96.8, and 71.9 percent, respectively. When defect levels increase to 133 defects per million inches, as shown for the 5-mil conductor in the figure, predicted yields drop to 98.7, 87.5, and 26.5 percent for 100, 1000, and 10000 inches of conductor, respectively.

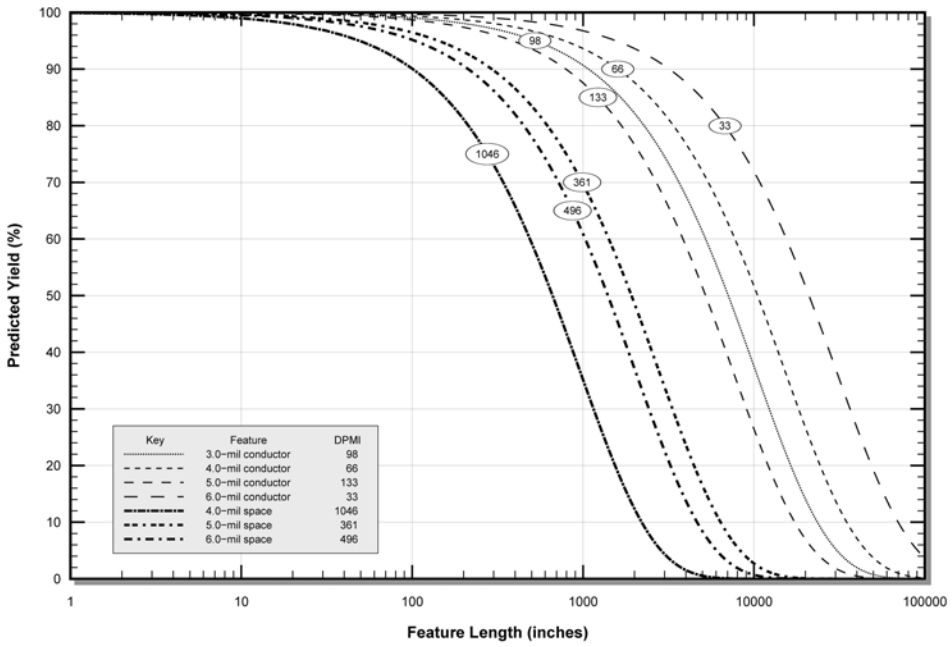

Figure 4. Predicted product yield versus conductor length.

Also shown in the figure is predicted product yield due to shorts between conductors versus space length on product. Defect densities in this example are higher for spaces than for conductors. The 5-mil space recorded a defect density of 361 defects per million inches of spaces. Once again, predicted yield falls off with increased space length on product for a fixed defect density.

To estimate the combined effects of opens and shorts on product yield, the fraction yield due to opens is multiplied by the fraction yield due to shorts and converted back to a percentage by multiplying by 100. As an example, if there were 1000 inches of 5-mil conductors and 500 inches of 5-mil spaces on product, the predicted yield would be 0.968 * 0.835 * 100 = 80.8 percent.

Given that conductors were fabricated successfully, their quality may be characterized by examining the accuracy and precision with which they were formed. Figure 5 displays the distributions of conductor width, space width, and conductor height, plotted versus feature size for 3-, 4-, 5-, and 6-mil outerlayer conductors, and 4-, 5-, and 6-mil spaces. The distributions are portrayed by notched box plots with the dashed lines showing the upper and lower specification limits; ± 20 percent in this example. When the conductors are formed accurately, the notched box plots are centered between the upper and lower specification limits. When the conductors are formed precisely, the distribution of widths indicated by the notched box plot will be tightly clustered. In this example, the median conductor widths were approximately 1.0 mil narrower than the target conductor widths, whereas the median space widths were approximately 1.0 mil wider than target.

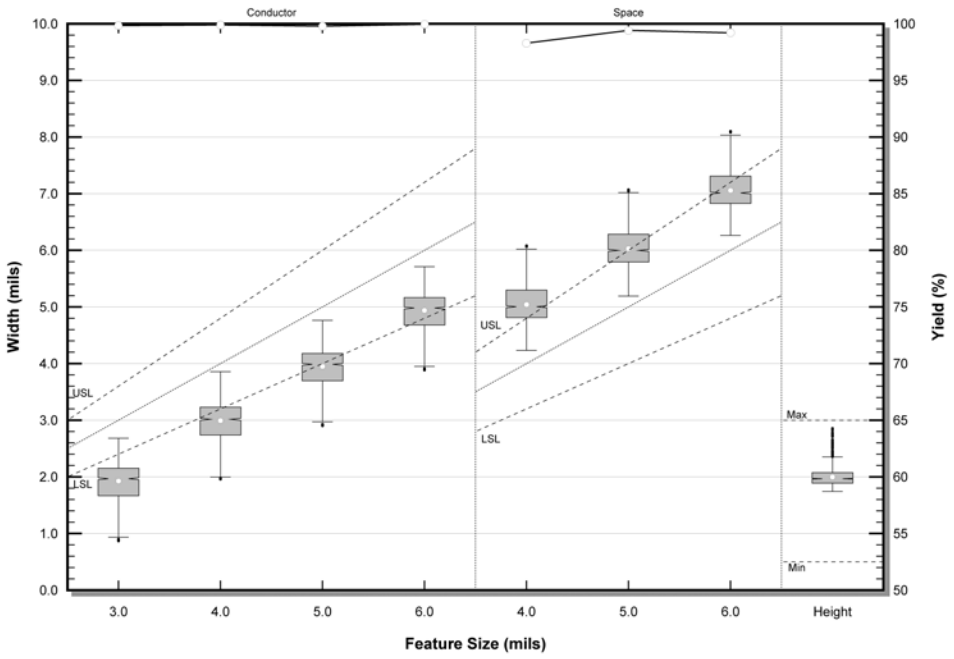

Figure 5. Measured conductor and space width versus target conductor width.

The quality of conductors is also affected by the accuracy and precision of their height. Figure 5 also shows the distribution of conductor height. In this example, nearly 1800 measurements were collected from 15 process capability panels. The mean conductor height was 2.0 mils, with a standard deviation of 0.15 mils.

Notice that the conductor height distribution has many outside values, as indicated by the dots above the upper adjacent value of the box plot. This data may be explained by examining panel-to-panel variation, shown in Figure 6. Conductor height (including plating thickness) of panel number 7 was much greater than that of the other panels.

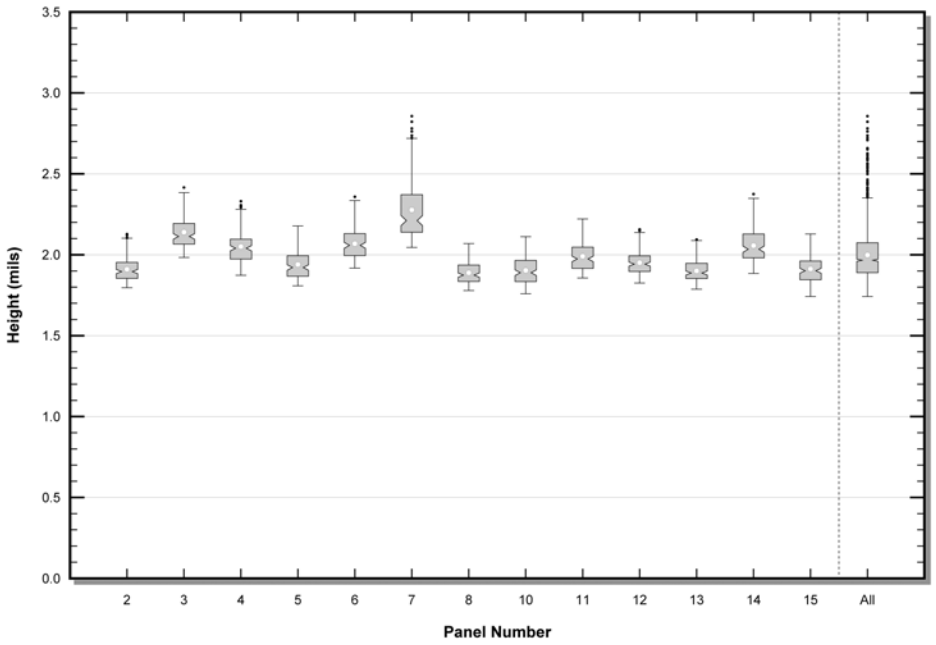

Figure 6. Conductor height versus panel number.

VIA CAPABILITY, QUALITY, AND RELIABILITY

The capability to form vias, and the quality and reliability of the interconnection depend upon many steps, including the registration, drilling, cleaning, metallization, and patterning processes. Misregistration of the via with respect to the pad(s) can lead to marginal interconnections that exhibit increased resistance and perhaps lead to reliability problems.

Registration capability of through vias is shown in Figure 7, which displays registration yield plotted versus radial distance. The smallest clearance (-1 mil), included to verify that the proper hole size was drilled, is intentionally designed to fail. Registration yield increased from 10 percent for the 3-mil designed clearance to 100 percent for the 8-mil clearance. If breakout were not allowed, then designs fabricated by the supplier in this example would require annular rings equal to or greater than 8 mils for the through vias. By designing to 5-mil annular rings, the data indicate that 35 percent of the through vias would exhibit breakout.

The capability to form through vias is shown in Figure 8, which displays predicted product yield due to opens in vias plotted versus the number of vias. Similar to predicted product yield for conductors and spaces, the estimated yield for a given defect density drops off with an increased number of vias in the design. For example the 10-mil vias recorded a defect density of 59 defects per million vias. At this defect level, the estimated yield drops from 94.3 percent to 55.4 percent by increasing the number of vias from 1000 to 10000.

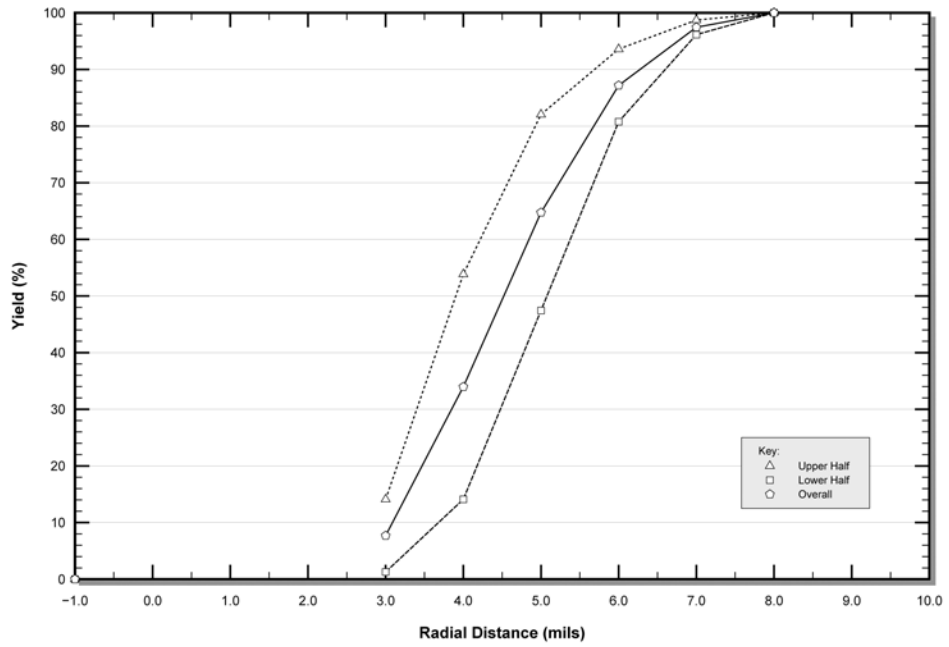

Figure 7. Via registration yield versus radial distance.

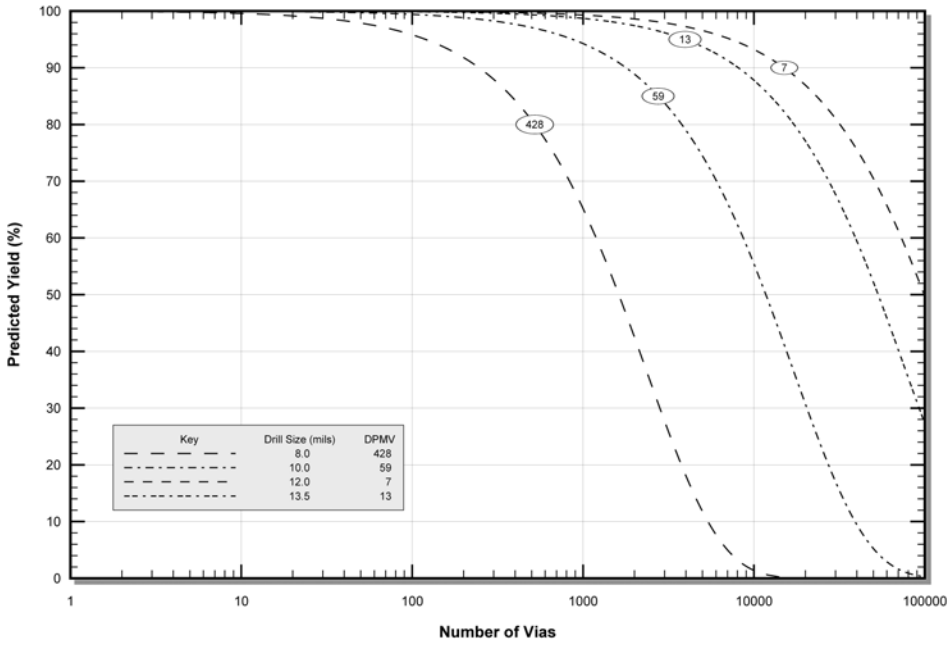

Figure 8. Predicted product yield versus number of vias.

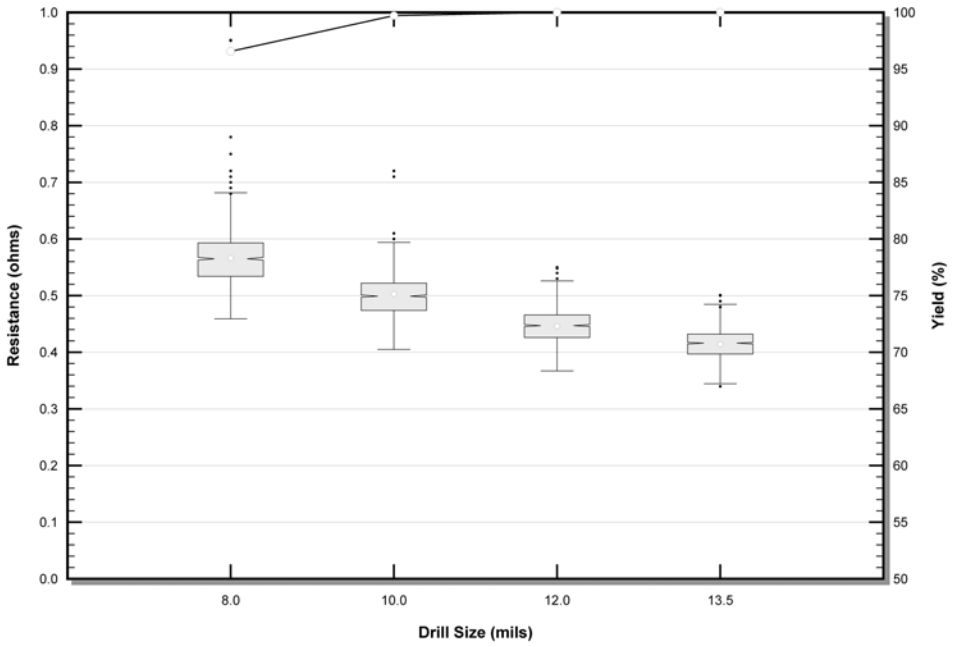

Figure 9. Via net resistance versus drill size.

The quality of vias may be investigated by examining the distribution of resistance measurements made from daisy chain patterns. Figure 9 shows the distributions for 8.0-, 10.0-, 12.0-, and 13.5-mil through vias. The results indicate that 12.0- and 13.5-mil diameter vias were fabricated with reasonably high quality, while the 8.0-mil and 10.0-mil diameter through vias exhibited poorer quality, as indicated by the broader distributions and numerous outside values.

Via reliability may be investigated by exposing the via daisy-chains to repeated thermal excursions, which accelerate failures that may occur in finished product while operating under normal conditions. The temperature changes impart tensile, compressive, bending, and shear stresses on the interconnect structure, caused by a mismatch in thermal coefficient of expansion between the metallic and dielectric materials. Further, material degradation may occur at elevated temperatures, which alter material properties and shorten expected life.

Samples that were subjected to 500 highly accelerated thermal shock (HATS) cycles from –40 to +145°C are shown in Figure 10. The failure distributions are depicted by notched box plots, with the median centered at the notch, and the box extending from the 25th percentile to the 75th percentile. The cycles to failure (as determined first by a 10 percent change in resistance, and then by an open circuit) are plotted for each of the four through-via sizes in the design.

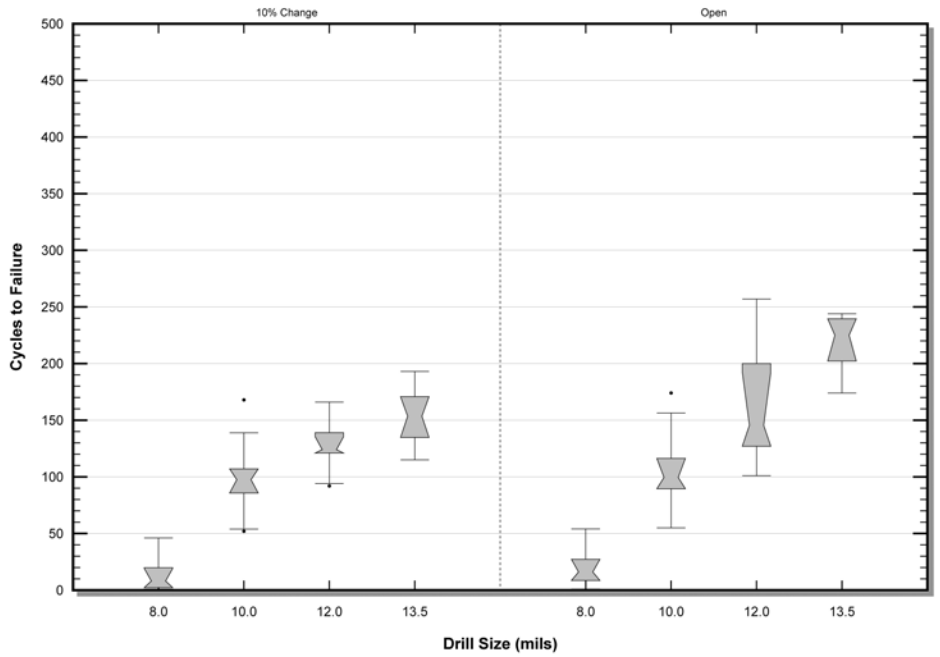

Figure 10. Cycles to failure versus drill size.

Figure 11 displays the thermal cycling results from the 13.5-mil diameter vias. Change in resistance, expressed in percent, is plotted versus cycle number. The figure shows that all the 13.5-mil daisy-chain nets exceeded 10 percent change prior to 200 cycles.

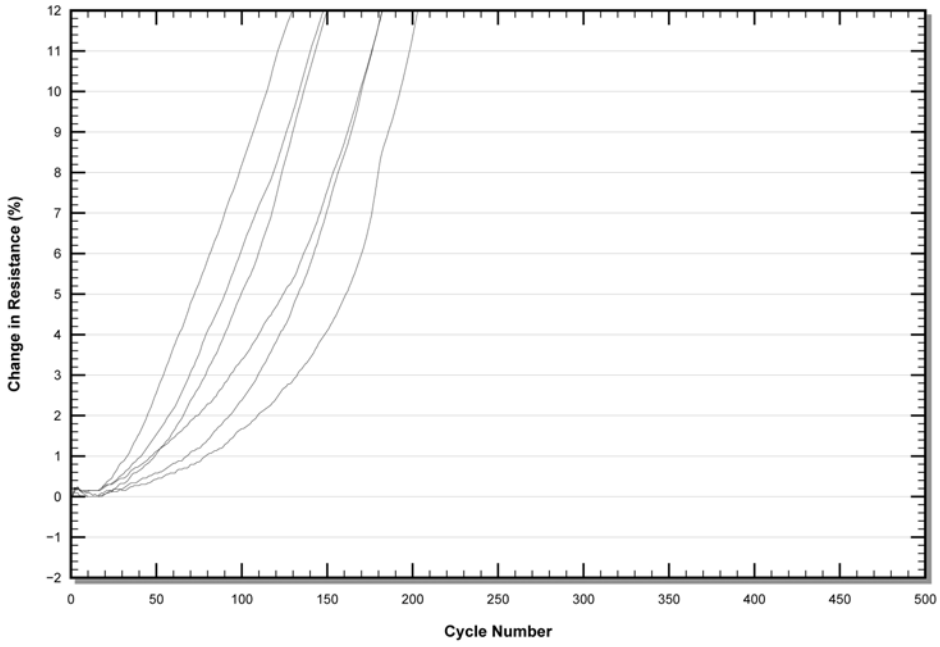

Figure 11. Via net change in resistance versus cycle number.

Further analysis of the data reveals additional information. In this example, the failure data are fitted to a Weibull distribution using a two-parameter log-likelihood model. Figure 12 shows cumulative failure probability plotted versus cycles to failure. The Weibull fit is indicated by the dashed line in the graph. Also indicated in red are 90-percent double-sided confidence bounds which were determined by the likelihood ratio and contour plots method. From the analysis, the shape parameter β is equal to 6.56, indicating wear out life, and the scale parameter η is 164.7. The mean time to failure for the 13.5-mil drilled through holes in these coupons was 153 cycles.

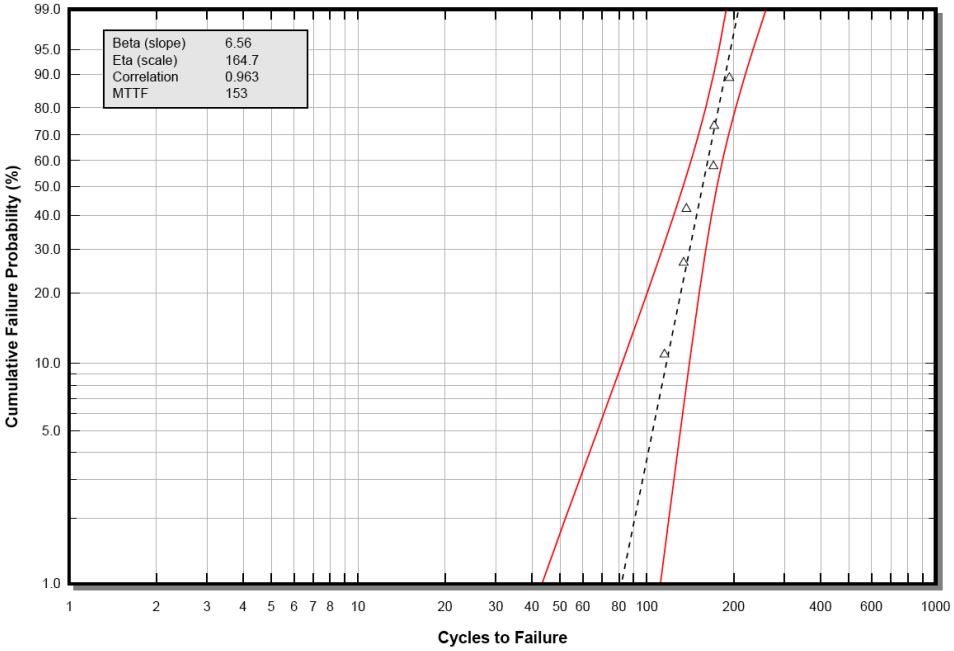

Figure 12. Cumulative failure probability versus cycles to failure.

SOLDER MASK REGISTRATION CAPABILITY

The solder mask prevents shorting between pads during the assembly process and protects surface features from mechanical and environmental damage. Registration of solder mask becomes increasingly important as surface-mount and ball grid array pitch sizes decrease. Therefore, the solder mask must be applied and patterned to stringent tolerances.

Results from solder mask registration data are shown in Figure 13, with clearance yield plotted versus radial distance. The clearances ranged from 1 to 3.5 mils in half-mil increments to provide a range of clearances that establish local registration. The clearance yield at 3.5 mils is 100 percent in this example. The yield falls off gradually to 2.5 mils, and then drops more significantly at smaller radial distances. The data from this process indicate that a clearance equal to or greater than 3.5 mils is necessary to ensure clearance between the solder mask and copper pads.

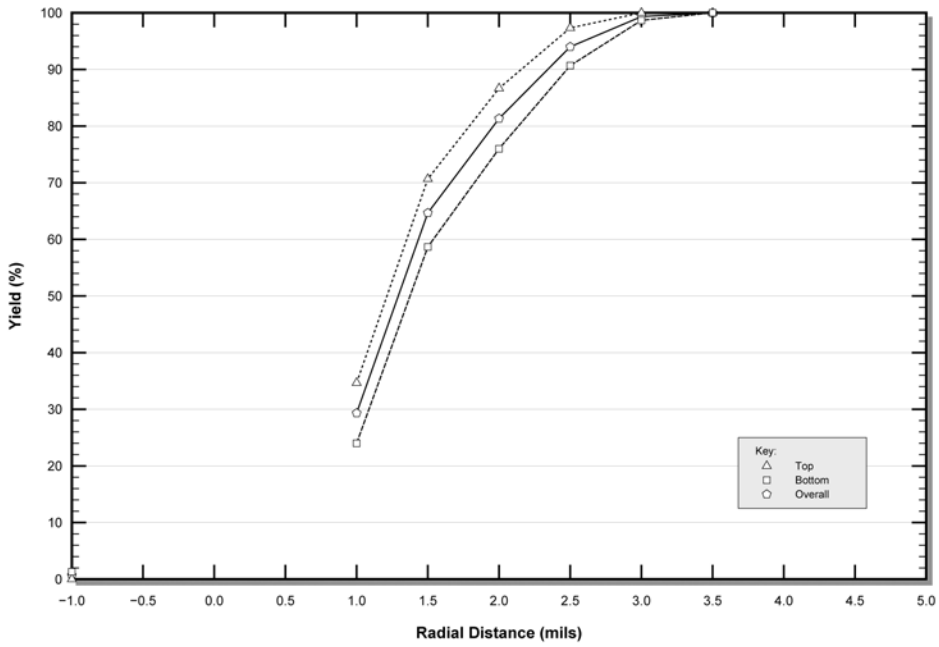

Figure 13. Solder mask clearance yield versus radial distance.

CONTROLLED IMPEDANCE CAPABILITY

Many applications require controlled impedance conductors for critical signals to ensure signal integrity. The impedance of a structure is primarily affected by the dielectric constant, the width and height of the conductor, and the separation between the conductor and the ground plane(s). After the dielectric materials are selected for a design, process variations that affect the conductor width and height, and distance to plane(s) impact the quality of the impedance structure.

Data collected from single-ended and differential surface microstrips are shown in Figure 14. The 50- and 100-ohm distributions are estimated from the 4-, 5-, and 6-mil trace results. Further analysis indicates that a 5.3-mil trace width would be required to achieve the 50-ohm single-ended microstrip, and 4.3-mil trace widths would be required to achieve the 100-ohm differential microstrip.

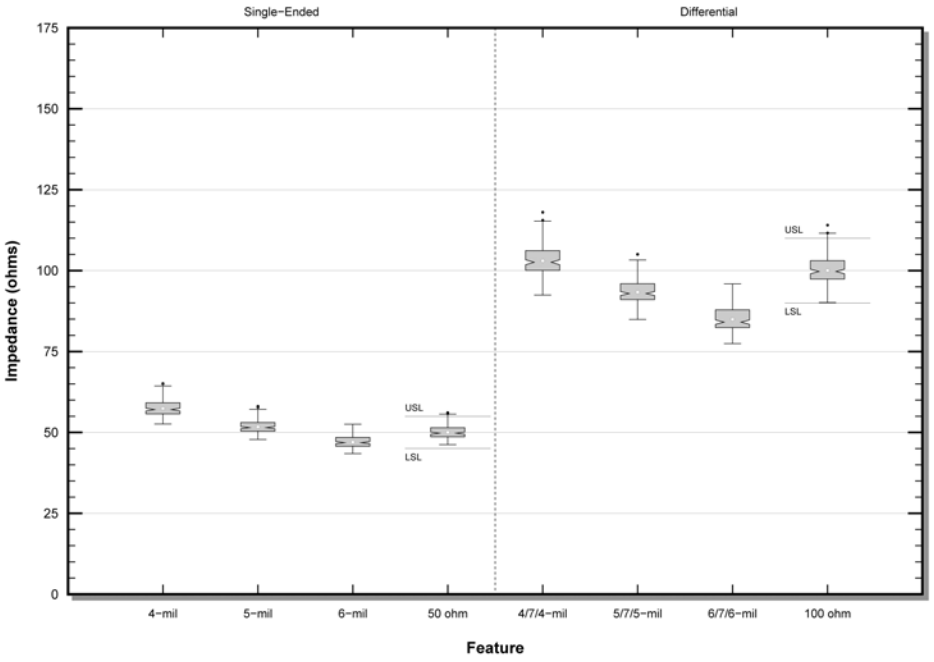

Figure 14. Single-ended and differential impedance versus feature size.

INDUSTRY STANDARDIZATION

Traditionally, purchasers of printed circuit boards have required that their suppliers demonstrate capability to fabricate their products, either by providing product samples for evaluation or by fabricating custom-designed test patterns for evaluation. The drawback to this approach is that each printed circuit board fabricator is required to produce unique samples for each of their customers. The time, materials, and resources used to fulfill these requests are significant since each customer requires different samples. Furthermore, the uniqueness and limited statistical relevance of each request make it difficult to compare the capability of a given supplier over time or to compare the capability of one supplier to another.

To establish industry standardization, in 2001 IPC formed the D-36 Subcommittee, "Printed Board Process Capability, Quality, and Relative Reliability Benchmark ($PCQR^2$) Test Standard and Database." The committee members developed a family of process capability panel designs, and established a database for the test results. The database consists of relevant statistics that characterize the capability of printed circuit board fabricators, and quantify the quality and reliability of their products.

The standardization has led to a minimal set of process capability panel designs, and has reduced the burden on fabricators to produce test samples by sharing data. Further, the database provides a direct comparison of one fabricator to another. By utilizing this industry-developed database, designers, purchasers, and assemblers of printed circuit boards can statistically benchmark their board suppliers' capabilities, make intelligent sourcing decisions, find and select new suppliers, ensure design for manufacturability, and establish realistic design rules.